

Faculty Mission: Enable 49 ML & AI Solutions

That 1.4 Billion People Are Waiting For

Where Intelligent Software Meets Designed-and-Built-in-India Hardware

Appendix G: CSE–ECE Co-Creation Framework

Because Half a Brain and Half a Body Never Built Anything Deployable

G-1 Ownership · G-2 Failure Modes · G-3 Curriculum · G-4 Project Structure · G-5 Assessment · G-6 Lab Setup · G-7 Faculty Roles · G-8 Objections · G-9 Case Study · G-10 Industry

For: All Faculty · HODs · Anyone Who Has Watched Two Excellent Department Projects Fail to Connect

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Why This Appendix Exists

This appendix is the most actionable section in the entire reference guide.

Everything in Appendices A through F described what needs to be built and how to build it right.

This appendix describes who builds it.
And how two departments — that have never shared a project, a lab or an assessment — begin doing so.

The framework here requires:

- No curriculum committee approval to start
- No additional budget to initiate
- No MOU to sign before beginning
- One conversation between two faculty members
- One shared project
- One shared assessment

That is all. Everything else follows from that.

Section	Content
G-1	Who Owns What — The Complete Ownership Map
G-2	What Breaks When They Don't Collaborate — 10 Real Failure Modes
G-3	The Joint Curriculum Model — Semester by Semester
G-4	The Joint Project Structure — How to Run One
G-5	The Shared Assessment Framework
G-6	The Co-Creation Lab Setup
G-7	Faculty Roles in Co-Creation — ECE and CSE
G-8	Overcoming Institutional Resistance
G-9	Case Study — What a Successful Joint Project Looks Like
G-10	The Industry Co-Creation Model

G-1: Who Owns What — The Complete Ownership Map

<u>ECE OWNS</u>	<u>SHARED — BOTH OWN</u>	<u>CSE OWNS</u>
Sensor selection	System architecture	ML model training
Sensing material spec	Power budget	Cloud platform
Excitation design	Link budget	Mobile application
PCB schematic	Data schema design	Government API integration
PCB layout	Edge vs cloud decision	Data pipeline
RF trace design	Sensor data trust chain	Dashboard + visualisation
Antenna selection	End-to-end test plan	Security architecture
Antenna placement	Deployment planning	OTA update mechanism
VSWR measurement	Field failure analysis	Data privacy compliance
Power supply design	Certification planning	User experience design
LDO/DCDC selection	BOM finalisation	Offline-first architecture
Battery/solar design	Manufacturing readiness	ML inference optimisation
EMC pre-compliance	IP rating specification	API error handling
Component specification	Connector selection	Database design
ESD protection design	Thermal specification	RTOS task design (with ECE)
Enclosure mechanical	Pre-compliance testing	Edge Impulse model (with ECE)
IP rating design	System integration test	Firmware data handling
Calibration methodology	Performance benchmarking	Alert + notification logic
Sensor lifetime tracking	Regulatory compliance	Multi-language interface
Hardware test procedure	Industry partner liaison	Government portal integration

The Shared Zone — Why It Is the Most Critical

The shared zone is where every IoT product succeeds or fails.

System architecture: CSE wants microservices on cloud. ECE says connectivity is intermittent. Together they design offline-first edge architecture. Neither alone gets it right.

Power budget: ECE designs STM32U5 in ULP mode — 13nA sleep.

CSE writes firmware that polls server every second. Sleep current becomes 80mA.

Battery life: 2 days instead of 2 years. Together they design sleep + wake cycle correctly.

Link budget: ECE selects LoRa antenna — 2 dBi gain. CSE sets SF7 for maximum data rate.

Range: 800m in urban area. Together they trade SF for range — SF12, 5 km. Problem solved.

Data schema: CSE designs JSON payload — 2 KB per message.

LoRa maximum payload: 242 bytes at SF12. Message does not fit.

Together they design compact binary payload — 18 bytes. Problem solved.

The shared zone decisions affect every layer above and below.

They must be made together. In the same room.

Before the first schematic is drawn or the first line of code is written.

The Ownership Decision Tree

Is this decision primarily about:

Physical matter (PCB, component, enclosure, antenna, sensor)?

└─ ECE owns – CSE must understand the constraint

Data and logic (algorithm, API, protocol, ML model, database)?

└─ CSE owns – ECE must understand the capability

Both physical AND data (power budget, link budget, data schema, system architecture, calibration trust chain)?

└─ BOTH own – neither can decide without the other

└─ Decision is made in joint design review – documented

If you find yourself making a shared-zone decision alone:

STOP.

Call the other department.

One email. One meeting. Get both perspectives. Then decide.

G-2: 10 Real Failure Modes — Every One Caused by Departments That Never Talked

FAILURE MODE 1: The ML Model That Learned the Sensor's Error

What happened:

CSE team trains soil moisture ML model on lab data. ECE team uses ₹50 sensor with DC excitation. Sensor drifts 15% over 3 months. ML model trained on drifted data — learns the drift as a feature. Model deployed in field — recommends wrong irrigation. Farmer loses crop.

Who should have caught it:

ECE — specify AC excitation + calibration in sensor spec

CSE — validate sensor data quality before training

Together — define data quality acceptance criteria

FAILURE MODE 2: The Battery That Lasted 2 Days

What happened:

ECE selects STM32U5 — 13nA sleep current. Calculates 2-year battery life on 3000 mAh cell. CSE writes firmware: MQTT connection every 60 seconds. MQTT keep-alive holds radio on continuously. Actual current: 12mA average. Battery life: 10 days.

Who should have caught it:

ECE — specify sleep current budget to CSE in shared document

CSE — measure actual current with PPK2 during development

Together — define power state machine before firmware begins

FAILURE MODE 3: The LoRa That Reached 200 Metres

What happened:

ECE places chip antenna on board. Does not measure VSWR. CSE sets SF7 (fastest data rate). System tested in college lab — works at 50m. Deployed in field — 200m range. Expected 5 km.

Who should have caught it:

ECE — measure VSWR of antenna in final assembly

ECE — verify antenna keepout zone in PCB layout

CSE — understand spreading factor vs range trade-off

Together — calculate link budget before hardware design freeze

FAILURE MODE 4: The Product That Cannot Be Legally Sold

What happened:

Team builds smart energy meter prototype. Demo works — project passes. Startup formed. DISCOM asks for BIS IS 16444 type approval number. Team has no certification. BIS process: 6 months + ₹3 lakh. DISCOM moves to imported meter.

Who should have caught it:

ECE — identify BIS IS 16444 in design phase

CSE — include certification plan in project plan

Together — certification planning document — mandatory before project approval

FAILURE MODE 5: The API That Only Works With WiFi

What happened:

CSE team builds ABDM-integrated RPM platform. REST API calls — 50KB response per vitals upload. ECE team uses NB-IoT — 200 kbps maximum. API response time: 30 seconds on NB-IoT. Timeout. Connection drops. Data lost.

Who should have caught it:

CSE — understand NB-IoT bandwidth constraints from ECE

ECE — specify connectivity constraints to CSE in week 1

Together — design API payload for constrained connectivity — binary protocol or MQTT

FAILURE MODE 6: The Sensor That Corroded in 3 Weeks

What happened:

ECE team uses bare copper electrodes for soil moisture sensor. CSE team builds beautiful dashboard. Demo day: works perfectly. 3 weeks later: copper electrodes corroded by soil chemistry. Readings: 0% moisture in flooded field.

Who should have caught it:

ECE — specify SS316L electrodes — sensing material science (Appendix C-4)

ECE — specify AC excitation — prevent electrolysis (Appendix C-5)

CSE — implement drift detection on dashboard — flag anomalous readings

FAILURE MODE 7: The Device That Interfered With Itself

What happened:

Board has WiFi (2.4 GHz) + LoRa (866 MHz). ECE places both antennas 15mm apart on same edge. WiFi transmit desensitises LoRa receive. When WiFi active — LoRa range drops 80%. CSE: 'Why does LoRa stop working when we upload data?' Root cause: $S_{21} = -8$ dB — insufficient isolation.

Who should have caught it:

ECE — measure S_{21} between antenna ports (Appendix D-5)

ECE — minimum spacing $\lambda/4 = 86$ mm between LoRa and WiFi antennas

CSE — test all radios simultaneously — not sequentially

FAILURE MODE 8: The Firmware That Failed in Monsoon

What happened:

CSE team writes firmware on desktop PC. All network calls assume stable WiFi. No error handling for failed connections. No local storage for offline periods. Device deployed in rural Maharashtra —

intermittent connectivity. Every connection failure: device reboots. Data loss: 60% of readings never reach cloud.

Who should have caught it:

ECE — specify connectivity profile to CSE — intermittent, not always on

CSE — implement offline-first architecture — store and forward

Together — define system behaviour for every connectivity state

FAILURE MODE 9: The Enclosure That Failed in First Rain

What happened:

ECE designs PCB — no thought to enclosure. CSE writes firmware — no thought to enclosure. 3D printed ABS box — no IP rating. First field deployment: Kerala monsoon. 48 hours: water ingress. Short circuit. Dead device.

Who should have caught it:

ECE — IP rating specification from day 1 — not week 12

ECE — cable entry glands — sealed connectors

CSE — firmware: detect power anomaly, log before failure

Together — enclosure design review before PCB layout finalised

FAILURE MODE 10: The Data Nobody Trusted

What happened:

Team builds river water quality system. Deploys in Yamuna river. CPCB reviews data — asks: 'Which NABL lab calibrated your sensors?' Team: 'We bought sensors from Amazon.' CPCB: 'This data has no authority. We cannot use it.' 6 months of data. Zero regulatory value.

Who should have caught it:

ECE — NABL calibration requirement — before sensor procurement

CSE — data provenance on dashboard — calibration metadata with every reading

Together — data authority framework — defined before deployment

Every one of these 10 failures has the same root cause:

Two departments made decisions independently that required the other's knowledge to get right.

The solution is not more knowledge.

It is more conversation.

Earlier in the project.

With both departments in the same room.

G-3: Joint Curriculum Model — Semester by Semester, Year by Year

Year 1 — Mutual Awareness (No joint project yet — plant the seed)

ECE Year 1 — Addition:

In digital electronics / basic circuits lab: one experiment per semester where students write Python code to analyse circuit measurements — plot I-V curves, FFT of signals.
CSE involvement: zero. But ECE students learn that code is a tool.

CSE Year 1 — Addition:

In programming lab: one project where students read data from a physical sensor (Arduino + temperature sensor + Python serial read).
ECE involvement: zero. But CSE students touch hardware.

Joint activity Year 1:

One guest lecture from ECE faculty to CSE class — 'What is inside your phone's hardware'
One guest lecture from CSE faculty to ECE class — 'What software does in embedded systems'
Timeline: Semester 2 — before Year 2 projects begin

Year 2 — First Contact (One shared experiment — not yet a project)

Semester 3 — Shared Lab Experiment:

ECE students: design a sensor circuit on breadboard, output to serial
CSE students: read serial data, process in Python, display graph
Both in same lab session — 3 hours — one outcome
Faculty from both departments present

Deliverable: Working sensor → Python graph — in 3 hours
Assessment: Each department assesses their own students
Learning: CSE understands hardware constraints.
ECE understands software potential.
Both understand: together = more than separately.

Semester 4 — First POC co-design:

ECE + CSE student pairs (one each) — assigned together
Task: ESP32 sensor node → MQTT → ThingSpeak dashboard
ECE owns: sensor + ESP32 hardware + antenna
CSE owns: firmware + MQTT + dashboard
Shared: power budget + data schema
Timeline: 4 weeks
Assessment: joint — both faculty evaluate both components

Year 3 — First Real System (Joint project — shared assessment)

Option A (ideal): New joint course

'IoT System Design' — 3 credits

Co-taught by ECE + CSE faculty

Mixed ECE + CSE teams of 4 (2+2)

One semester — one system — both departments assess

Option B (practical — no new course needed):

ECE final year lab + CSE project course — coordinated

Same problem statement — different deliverables — joint integration

Same demo day — both faculty present — joint assessment

Year 3 Project Requirements

- 4-layer PCB — not breadboard — not dev board
- NABL-calibrated sensor — not online ₹50 sensor
- RTOS firmware — not Arduino loop
- One government API integrated — tested with sandbox credentials
- Power budget calculated + measured with PPK2
- Link budget calculated + range verified in real environment
- Architecture document — shared, signed by both ECE and CSE team members
- Joint assessment — both departments evaluate all components

Year 4 — Product Engineering (Full co-creation — industry jury)

Team structure:

4–6 students — minimum 2 ECE + 2 CSE

One project supervisor from ECE + one from CSE

External industry mentor — from IoT company or government agency

Year 4 Deliverables — ALL Mandatory

- Working 4-layer PCB product — EMC pre-compliance tested
- IP67 field-tested enclosure — 48-hour outdoor exposure minimum
- NABL-calibrated sensor — with sensor health on dashboard
- Production firmware — RTOS + OTA + error logging + offline-first
- Live government API integration — real credentials — not sandbox
- Certification plan document — BIS/WPC/TEC/CDSCO as applicable
- Manufacturer-ready BOM — authorised distributors only
- Test procedure document — factory test for each unit
- Field trial report — minimum 4 weeks in real conditions

□ Grant application — one scheme applied for (DST NIDHI, TIDE 2.0, etc.)

Assessment:

40% ECE faculty — hardware quality

40% CSE faculty — software quality

20% External industry jury — 'Would you deploy this?'

Total: 100% — joint score — both departments sign off

The Semester-by-Semester Timeline — At a Glance

Semester	ECE Activity	CSE Activity	Joint Activity
S1	Electronics basics	Python + basics	Guest lecture (mutual)
S2	Sensors + circuits	Arduino basics	Guest lecture (mutual)
S3	Sensor circuits lab	Python data lab	Shared sensor → graph experiment
S4	ESP32 hardware	ESP32 firmware	First POC co-design pair project
S5	STM32 + PCB design	STM32 firmware + MQTT	Joint system design — same problem
S6	4-layer PCB + LoRa	RTOS + cloud + API	Joint project — architecture document
S7	EMC pre-compliance + SOM	Edge ML + government API	Joint capstone begins
S8	Enclosure + field trial	Production firmware + OTA	Joint capstone deliverable + jury

G-4: The Joint Project Structure — How to Run One

The Joint Project Charter — Template

PROJECT CHARTER

PROJECT TITLE: _____
SOLUTION ID: _____ (from Appendix A)

TEAM COMPOSITION:

ECE Students: _____ + _____
CSE Students: _____ + _____
ECE Supervisor: _____
CSE Supervisor: _____
External Mentor: _____ (optional)

PROBLEM STATEMENT:

[Specific Indian problem this project solves]
[Scale: how many people / how much impact]
[Why existing solutions don't work]

SYSTEM ARCHITECTURE (agreed before any design begins):

Perception: [Sensors + sensing principle + material + excitation]
Network: [RF technology + link budget + frequency]
Processing: [MCU + MPU + edge AI – which and why]
Application: [Platform + APIs + dashboard + ML model]

SHARED DECISIONS – BOTH TEAMS SIGN:

Power budget:

Sleep current target: _____ μ A (ECE designs to, CSE codes to)
Active current target: _____ mA
Battery capacity: _____ mAh | Target battery life: _____ months

Link budget:

TX power: _____ dBm | Antenna gain: _____ dBi
Target range: _____ km | Spreading factor: _____

Data schema:

Payload format: [binary / JSON / CBOR – agreed]
Payload size: _____ bytes (must fit RF MTU)
Update frequency: _____ seconds

Sensor calibration:

Calibration method: _____ | NABL lab: _____

ECE DELIVERABLES – with deadlines:

- Schematic – Week ____
- PCB layout (4-layer) – Week ____
- PCB order – Week ____
- Hardware assembly – Week ____
- VSWR measurement – Week ____
- PPK2 power measurement – Week ____
- EMC near-field scan – Week ____
- IP67 enclosure – Week ____

CSE DELIVERABLES – with deadlines:

- Architecture document – Week ____
- RTOS firmware structure – Week ____
- Cloud platform + API sandbox – Week ____
- Edge ML model (Edge Impulse) – Week ____
- Dashboard + alerting – Week ____
- Offline-first firmware – Week ____
- OTA update mechanism – Week ____
- Data privacy compliance – Week ____

JOINT DELIVERABLES:

- System integration test – Week ____
- End-to-end field test – Week ____
- Certification plan – Week ____
- Final report – Week ____

SIGNATURES (before work begins):

ECE S1: _____ Date: _____
 ECE S2: _____ Date: _____
 CSE S1: _____ Date: _____
 CSE S2: _____ Date: _____
 ECE Supervisor: _____ Date: _____
 CSE Supervisor: _____ Date: _____

The Joint Project Timeline — 16 Weeks

Week	ECE Milestone	CSE Milestone	Joint Milestone
1	Problem analysis + sensor research	Problem analysis + API research	Project charter signed
2	Sensor selection + spec + calibration plan	Architecture + data schema	Architecture document signed
3	Schematic design begins	Firmware skeleton + RTOS structure	Power budget agreed
4	Schematic complete — ECE review	Cloud platform + sandbox API	Link budget agreed
5	PCB layout begins (4-layer)	MQTT + data pipeline	Data schema agreed
6	PCB layout complete — DRC	Edge Impulse model — first iteration	PCB design review — both departments
7	PCB ordered — JLCPCB/Shogini	Firmware — sensor reading + transmit	—
8	PCB arrives — assembly begins	Dashboard — first data display	First integration test on dev board
9	PCB assembled — basic test	API integration — sandbox complete	System integration on dev board — working
10	VSWR measurement — antenna tuning	ML model deployed on MCU	Power profiling — PPK2 measurement
11	EMC near-field scan — fix issues	OTA + offline-first complete	Full system test — lab
12	Enclosure design + 3D print	Government API — live credentials	Certification plan document
13	IP test — rain + dust exposure	Data privacy compliance check	Field deployment preparation
14	Field deployment — 2 weeks start	Field monitoring — data quality	Field trial week 1
15	Hardware field issues — fix	Software field issues — fix	Field trial week 2
16	Final hardware report	Final software report	Joint presentation + industry jury

G-5: The Shared Assessment Framework

Current practice: ECE faculty assess ECE deliverables — hardware marks.
 CSE faculty assess CSE deliverables — software marks.
 Neither department can assess the integrated system.
 Neither department feels responsible for the other's failures.

What this produces: Hardware that works in isolation but not with the software.
 Software that works on a laptop but not on the hardware.
 Integration is an afterthought — not a design goal.

What joint assessment produces:
 Both departments must care about both components.
 The product is the unit of assessment — not the component.
 Integration is a first-class deliverable — assessed directly.

The Joint Assessment Rubric

Component	Weight	ECE Marks	CSE Marks	Who Assesses
Hardware design quality	20%	20%	—	ECE faculty
Software design quality	20%	—	20%	CSE faculty
System integration	20%	10%	10%	Both faculty together
Field performance	20%	10%	10%	Both faculty together
Industry jury verdict	20%	—	—	External jury
TOTAL	100%			

Hardware Assessment Criteria — ECE Faculty Use

Criterion	0–4 (Poor)	5–7 (Acceptable)	8–10 (Excellent)
PCB stack-up	2-layer or no ground plane	4-layer — ground plane present	4-layer — impedance controlled — verified
Antenna	No VSWR measurement	VSWR measured — > 2:1	VSWR measured — < 1.5:1 in final assembly
Sensor integrity	No calibration	Calibration attempted	NABL certificate — drift monitoring in firmware
Power budget	Not calculated	Calculated — not measured	Calculated + measured with PPK2 — within 10%
EMC	No pre-compliance	Near-field scan done	Issues found + fixed — documented
Enclosure	No enclosure	3D printed — no IP test	IP67 — field tested — 48 hours

Criterion	0–4 (Poor)	5–7 (Acceptable)	8–10 (Excellent)
ESD protection	None	TVS on some connectors	TVS on all external pins — GDT on antenna
BOM	IndiaMART sources	Mixed sources	Authorised distributors only — with certificate

Software Assessment Criteria — CSE Faculty Use

Criterion	0–4 (Poor)	5–7 (Acceptable)	8–10 (Excellent)
RTOS structure	Arduino loop	FreeRTOS — basic tasks	FreeRTOS — tasks + queues + power states
Offline-first	No offline handling	Local storage — no retry	Store-and-forward — retry with backoff
API integration	API not integrated	Sandbox credentials	Live credentials — error handling complete
ML model	No ML	Browser-based model	On-device inference — inference time measured
Sensor health	Raw data only	Calibration date shown	Full sensor health — drift + lifetime + alert
OTA update	No OTA	OTA mechanism present	OTA tested — rollback on failure
Data privacy	No consideration	DPDP Act reviewed	Compliance documented + implemented
Power states	Always on	Sleep implemented	Sleep verified — PPK2 current matches budget

Integration Assessment Criteria — Both Faculty Together

Criterion	0–4 (Poor)	5–7 (Acceptable)	8–10 (Excellent)
Architecture document	Not present	Present — incomplete	Complete — signed by all team members
Power budget agreement	Not aligned	Partially aligned	Fully aligned — ECE design + CSE code match
Link budget agreement	Not calculated	Calculated — not verified	Calculated + RF range verified in field
Data schema	Mismatch — data doesn't fit RF	Fits RF — not optimised	Optimised binary — fits LoRa MTU
System integration test	Works in lab only	Works in lab + some field	Works in field — 4-week report
Certification plan	Not present	Identified certifications	Full plan — cost + timeline + lab identified

The Industry Jury Brief

What to tell the external jury:

'You are evaluating whether this product is deployable in India.

Not whether it is technically interesting.

Not whether the report is well written.

Deployable — legally, reliably and at scale.

Please answer three questions:

1. Would you deploy this in a real field application?

If no — what is the single most important thing to fix?

2. Is the hardware designed to survive Indian field conditions?

Dust, heat, monsoon, voltage fluctuations.

3. Is the software designed for Indian operational reality?

Connectivity gaps, multiple languages, government API integration.

Score: 20 marks. Your score is final — faculty cannot override it.

That is the point — we are preparing students for your world.'

G-6: The Co-Creation Lab Setup

A co-creation lab is not a new lab.

It is the ECE hardware lab and the CSE software lab with one shared workbench between them.

Physically:

Shared table: ECE student + CSE student — side by side

ECE side: oscilloscope, soldering station, NanoVNA, PPK2, multimeter

CSE side: laptop with STM32CubeIDE, Edge Impulse, KiCad, Node-RED

Centre: the board being built — belongs to both

Institutionally:

One lab slot — both departments blocked at the same time

Joint faculty availability — both present

One problem on the whiteboard — visible to everyone

The Minimum Co-Creation Lab — ₹1.5 Lakh

Item	Cost	Purpose
NanoVNA V2	₹3,000	Antenna VSWR measurement — ECE tool
Nordic PPK2 Power Profiler	₹4,000	Sleep current measurement — shared tool
Near-field probe set	₹3,500	EMC pre-compliance — ECE tool
FLIR ONE Pro thermal camera	₹15,000	Thermal analysis — shared tool
Rigol DS1054Z oscilloscope	₹28,000	Signal analysis — ECE tool
Hakko FX888D soldering station	₹6,000	PCB assembly — ECE tool
Hot air rework station	₹3,000	SMD rework — ECE tool
Laptop (for KiCad + STM32CubeIDE)	₹45,000	PCB design + firmware — ECE/CSE shared
Dev boards (starter set)	₹20,000	POC builds — both teams
Components + consumables	₹10,000	Resistors, caps, connectors, solder
TOTAL	₹1,37,500	

One DST FIST application covers 10 such workbenches.

One industry CSR donation covers 5.

One department budget covers 1.

Start with 1.

The Co-Creation Lab Rules

Posted on the lab wall — alongside the Engineering Mindset Pledge:

Rule 1: No ECE student leaves without CSE partner reviewing the firmware.

Rule 2: No CSE student leaves without ECE partner reviewing the power budget.

Rule 3: No project proceeds to PCB order without a shared architecture document.

Rule 4: No project passes without a VSWR measurement and a PPK2 measurement.

Rule 5: The ₹50 sensor is a POC tool. Not an engineering tool. Not in this lab.

Rule 6: Every decision that touches both hardware and software — both teams in the room.

Rule 7: The vendor delivers what you specify. Specify everything. Accept nothing less.

G-7: Faculty Roles in Co-Creation

Activity	ECE Faculty Role	CSE Faculty Role
Project selection	Identify hardware feasibility + sensor requirements	Identify API + data feasibility + ML possibility
Architecture review	Review power budget + RF design + sensor spec	Review data schema + API design + ML approach
Week 4 design review	Review schematic — decoupling, ESD, antenna	Review firmware structure — RTOS, power states
Week 6 PCB review	Review layout — ground plane, impedance, keepout	Review firmware — check data payload fits RF MTU
Week 10 integration	Measure VSWR + PPK2 — validate vs budget	Validate API response time on actual RF link
Week 14 field trial	Hardware field performance — failure analysis	Software field performance — data quality, uptime
Final assessment	Hardware rubric (20%) + integration (10%)	Software rubric (20%) + integration (10%)
Jury management	Brief jury on hardware — answer hardware questions	Brief jury on software — answer software questions

What Each Faculty Must Learn — Minimum

ECE Faculty — minimum CSE knowledge needed:

- What RTOS is and why it matters for power management
- What MQTT is and how it affects RF bandwidth
- What Edge Impulse does — how ML runs on STM32
- What government APIs exist for your domain — from Appendix A
- What DPDP Act means for student projects
- How to read a basic power profiler measurement from PPK2

CSE Faculty — minimum ECE knowledge needed:

- What a ground plane is and why it matters for EMC
- What VSWR is and what > 2:1 means for RF performance
- What link budget is — why SF7 gives different range than SF12
- What sensor calibration means — why ₹50 sensor is a POC tool
- How to read a near-field probe scan result — what a hotspot means
- What IP67 means — why it matters for field deployment

This is not advanced knowledge.

It is 4 hours of reading — from Appendices B, C and D.

Faculty who read those three appendices can mentor a co-creation project effectively.

The Faculty Co-Mentoring Rhythm

Week	Joint Faculty Action
1	Joint kickoff — both faculty, all students — architecture discussion
4	Joint design review — schematic (ECE) + firmware skeleton (CSE) — 90 minutes
6	Joint PCB review — layout (ECE) + data schema (CSE) — 60 minutes
8	Joint integration review — dev board system working? — 60 minutes
10	Joint power + RF review — PPK2 + VSWR — 60 minutes
12	Joint enclosure + API review — IP test planned? API live? — 45 minutes
14	Joint field deployment review — everything working? — 30 minutes
16	Joint final review + jury briefing — 90 minutes

Total faculty time per semester per joint project: ~10 hours each.

That is less than one hour per week.

For a deliverable that changes what India deploys.

G-8: Overcoming Institutional Resistance — The Objections and the Responses

Objection 1: 'Our timetables don't align'

The objection: ECE lab is Tuesday 2–5 PM. CSE lab is Thursday 9–12 AM. Students can't be in both.

The response: They don't need to be in both. They need to be in ONE shared session. Replace one ECE lab slot + one CSE lab slot with one joint session — same time, same room. Reduce two 3-hour sessions to one 4-hour joint session. Net saving: 2 hours of timetable for 4 hours of engineering.

Objection 2: 'Anna University regulation doesn't allow this'

The objection: Our curriculum is fixed by Anna University. We can't add new subjects without AU approval. Joint projects don't fit existing course structures.

The response: Internal assessment marks are faculty's discretion. Mini projects, seminars and electives are often flexible. A joint project doesn't need a new course — it needs a coordinator. One faculty member from each department agrees. Existing project hours are used — just with a shared problem. Anna University R-2021 has project-based learning components — these can be jointly supervised. No regulation approval needed. Just two faculty members and one HOD.

Objection 3: 'How do we allocate marks fairly?'

The objection: If ECE student and CSE student work together — how do I give separate marks to each? What if one does more work than the other?

The response: Use the rubric in G-5. ECE faculty assess hardware quality — only ECE student's work. CSE faculty assess software quality — only CSE student's work. Both assess integration — both students' shared work. Individual contributions are documented in architecture document. Each student has a defined ownership area — assessed independently. Fairness is in the design — not the aftermath.

Objection 4: 'ECE students don't know software, CSE students don't know hardware'

The objection: Our ECE students can't write MQTT firmware. Our CSE students don't know how to read a schematic. How can they work together?

The response: They don't need to know everything — they need to know enough to collaborate, not to replace each other. ECE student learns: RTOS basics, MQTT, Edge Impulse (4 hours of MOOC). CSE student learns: what a ground plane is, what VSWR means, what LoRa SF means (2 hours of reading Appendix B + D). The collaboration fills the gap — the gap is the feature, not the bug. A student who knows their own domain deeply and their partner's domain minimally is more valuable than one who knows both domains shallowly.

Objection 5: 'Industry doesn't ask for this — students just need coding skills'

The objection: Our alumni are placed in software companies. They don't need hardware skills. Why complicate the curriculum?

The response: That was true in 2015. The top-paying roles in 2025 are at the hardware-software boundary: Edge AI engineer: ₹15–40 LPA. Embedded AI engineer: ₹12–30 LPA. IoT solutions architect: ₹15–35 LPA. These roles require exactly the skills this curriculum develops. The alumni placed in pure software companies are competing with 1.5 million other graduates for the same roles. The alumni who can bridge hardware and software are competing with a global pool of < 50,000 engineers. The opportunity is at the boundary — not in the middle.

G-9: Case Study — A Successful Joint ECE–CSE Project

End to End

Project Name: Smart Grain Silo Monitoring System
Solution Reference: GR-1 (Appendix A-1)
Team: 2 ECE + 2 CSE students — Year 4 capstone
Duration: 16 weeks — one semester

Week 1–2: Architecture Agreement

ECE team researched:

Grain probe sensor material: SS316L electrodes for corrosion resistance
CO₂ sensor for fermentation detection: MH-Z19 NDIR — factory calibrated
Power: solar + LiPo — calculated 90-day autonomy
RF: STM32WL55 LoRa — India 866 MHz
Enclosure: IP65 — godown dust conditions

CSE team researched:



FCI FIMS API — found documentation at fci.gov.in
Spoilage prediction ML — ICAR research papers + temperature + CO₂ correlation
Dashboard: Grafana + InfluxDB — open source
Alert: WhatsApp Business API for FPS dealer SMS

Joint decisions:

Data schema: 18-byte binary payload (fits LoRaWAN SF12 MTU)
Power budget: 12 μ A sleep — verified achievable with STM32WL + solar
Link budget: SF12, 866 MHz, 2 dBi — 8 km in open — FCI depot to gateway
Architecture document: signed by all 4 students + both faculty supervisors

Week 3–8: Parallel Development

ECE milestones:

Week 3: Schematic — STM32WL55 + SS316L probe + MH-Z19 + solar MPPT
Week 4: PCB layout — 4-layer — ground plane — antenna keepout
Week 5: PCB ordered — JLCPCB 4-layer impedance controlled
Week 6: PCB arrived — assembly + basic test
Week 7: VSWR measurement — 866 MHz — 1.3:1 
Week 8: PPK2 measurement — sleep current 9.8 μ A 

CSE milestones:

Week 3: RTOS structure — FreeRTOS — sensor task + LoRa task + sleep task
Week 4: Cloud platform — InfluxDB + Grafana — first dashboard

Week 5: FCI FIMS API sandbox — credentials obtained, test calls working
Week 6: Edge Impulse spoilage model — trained on temperature + CO₂ data
Week 7: WhatsApp Business API — alert trigger working
Week 8: OTA update mechanism tested on dev board

Week 9–12: Integration

Week 9 joint test:

ECE hardware + CSE firmware — first integration on custom PCB.
Issue found: CO₂ UART conflicts with LoRa UART — IRQ timing clash.
ECE + CSE together: resolved with FreeRTOS mutex — 3 hours.

Week 10 power profiling:

PPK2 with full firmware: sleep 11.3µA (budget was 12µA)
Active with LoRa TX: 42mA peak — within solar charging design

Week 11 link budget verification:

Real-world LoRa range test — Coimbatore industrial area.
Gateway on 10m pole — measured range: 3.2 km (budget predicted 3.8 km)

Week 12 enclosure:

3D printed enclosure — fit check — all connectors accessible.
IP65 test: rain from garden hose — 30 minutes — no ingress
VSWR remeasured in enclosure: 1.6:1 (shift from 1.3:1 — still within spec)
Certification plan document: BIS CRS + WPC ETA — identified, cost estimated


Week 13–16: Field Trial and Assessment

Field deployment:

Device deployed in local rice mill cold storage area — 4 weeks.

FCI FIMS API: live test data uploaded (research mode).

Spoilage ML: detected 3 temperature excursion events correctly.

WhatsApp alert: sent to faculty mobile — received within 2 minutes of event 

Industry jury verdict:

Jury member: Senior engineer from a grain logistics company.

Hardware: 'I would deploy this. PCB is clean. VSWR is measured. IP65 is tested.'

Software: 'FCI integration correctly architected. WhatsApp alert is exactly right.'

Improvement: 'Sensor calibration certificate is missing — you have a sensor, not a calibrated instrument.'

Score: 16/20 — minus 4 for missing NABL calibration certificate.

Lessons applied:

NABL calibration booked for SS316L probe — certificate received week after submission.

Team noted: 'We will design calibration in from week 1 next time — not week 15.'

That learning is worth more than the 4 marks.

G-10: The Industry Co-Creation Model

Three things industry brings that college cannot:

1. Real problem specification

Industry has actual unsolved problems — not textbook problems.
A company deploying IoT in agriculture has data quality issues, sensor failure patterns, connectivity gaps — real, specific, solvable.

2. Field testing access

Students need to deploy in real conditions.
Industry partner provides: installation site, field access, real user feedback.

3. Post-graduation continuity

The best student projects become internships.
The best internships become employment.
The best employment becomes India's IoT product ecosystem.

How to Find Industry Partners

Source	How to Approach	What to Offer
Local MSMEs	Direct visit — offer to solve their machine monitoring problem	Free prototype + student labour + IP shared
State government departments	Through principal/management — offer pilot for agriculture/water scheme	Pilot data + student project report
IoT startups	LinkedIn + Hackster community — offer co-development	Student team + college resources
NASSCOM member companies	NASSCOM IoT community — formal partnership request	Joint publication + IP sharing
Anna University industry connect	AU has industry liaison office — use it	AU brand + student manpower
TiE (The Indus Entrepreneurs)	TiE Chennai — startup network	Student + faculty partnership
CII / FICCI	Industry associations — formal MOU	Research partnership

The Industry Partner Agreement — Minimum Terms

What the college provides:

- Student team (ECE + CSE) — 16 weeks
- Faculty supervision — 2 faculty members
- Lab access — hardware + software tools
- Institutional support — college name + facilities

What the industry partner provides:

- Problem statement — specific and real
- Field access — deployment site for 4-week trial
- Domain expert — available 2 hours/week for student questions
- Equipment or components — if specialised hardware needed
- Internship offer — for outstanding students post-project

IP arrangement:

- Student retains academic credit — college retains publication right
- Industry partner retains commercial rights to deploy the solution
- If student's work leads to commercial product — royalty arrangement (optional)

This does not require a formal MOU for pilot.

A one-page letter of understanding is sufficient to start.

Cross-References

For	Go to
The 49 solutions — which ones are joint Year 4 projects	Appendix A6: Master Solutions Index Year-Wise Guide
Hardware engineering the ECE team must deliver — PCB, antenna, sensor	Appendix C: Engineering Integrity C-11, C-12, C-19
Sensor integrity — calibration, material science — ECE team responsibility	Appendix C: Engineering Integrity C-4, C-5, C-6
Government APIs the CSE team must integrate — per domain	Appendix A1–A5: Solutions Matrix API tables per solution
VSWR measurement — NanoVNA guide — ECE tool for lab rule 4	Appendix D: Antenna Engineering D-7
PPK2 power profiling — shared tool for lab rule 2	Appendix C: Engineering Integrity C-19
Government schemes for the joint team to apply for — DST NIDHI, TIDE 2.0	Appendix F: India Hardware Ecosystem F-6
Edge Impulse + NPTEL courses — what CSE and ECE learn in MOOC hours	Appendix H: Learning Ecosystem