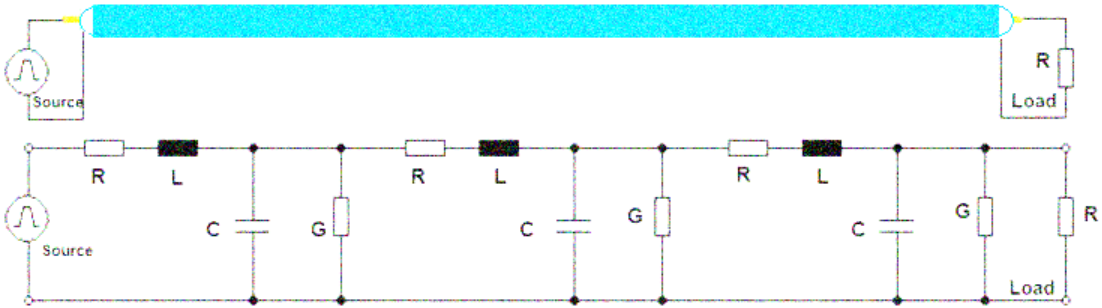
Engineering Fundamentals for PCB Layout Design



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"Guiding Curious Minds to Practical Engineering Solutions"

Feb 2026

Audience, Purpose and Pre requisites

Intended Audience:

- Students and Professionals from Electrical & Electronics or Instrumentation engineering, or anyone those who are involved in PCB Lay outing.

Purpose:

- To give the foundational engineering perspective on **1)** the parasitic elements of PCB traces such as Resistance “R”, Inductance “L” Capacitance “C” and conductance; **2)** the electromagnetic fields within the PCB; **3)** the Safety aspects and **4)** Thermal management aspects

Pre-requisites

- Basic knowledge about electrical & electronics components (Passives, Semiconductor discrete and ICs). Exposure to creating PCB layout using any software.

Details on this content & Request to the learner

This material is compiled by

https://www.seekerssignpost.com/

A Request to the Reader: If you like this content, and you want to share this to someone who may be benefited, *please share the weblink of this material.*

Note: This content uses references to some of the great materials out there on the internet from several component manufacturers and other websites etc., We humbly recognize and thank all of those efforts which brings clarity to engineers and help making the product development great.

In case if you are an owner of such content and for some reasons you do not want the references to be a part of these slides, please feel free to write an e-mail to us to remove those references. Also, you can send us your comments, feedback and nay new content requirement to our e-mail ID.

e-mail: seekerssignpost@gmail.com

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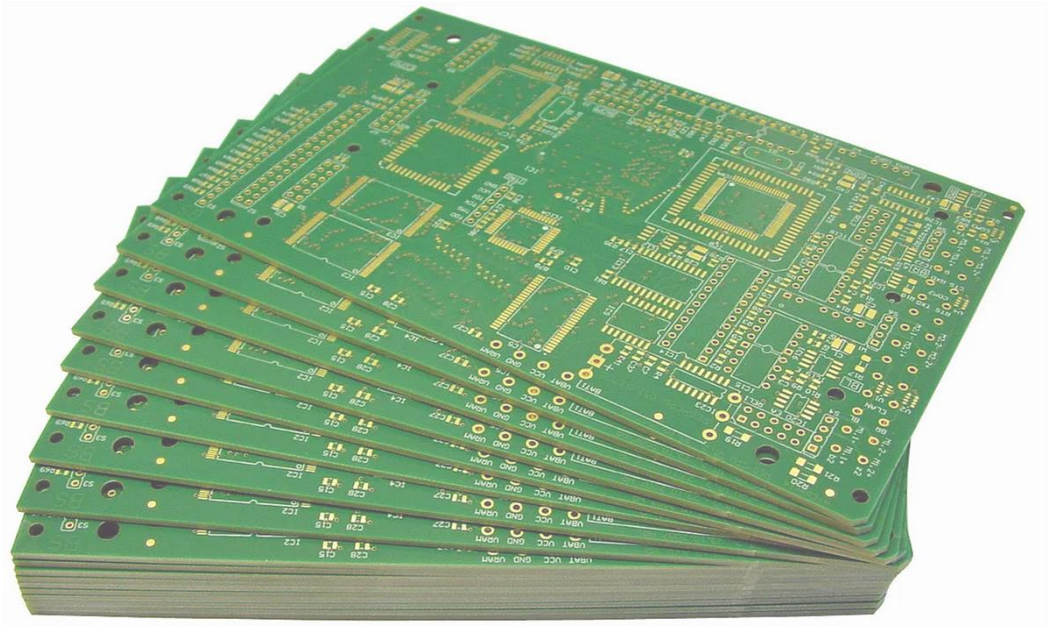
Introduction



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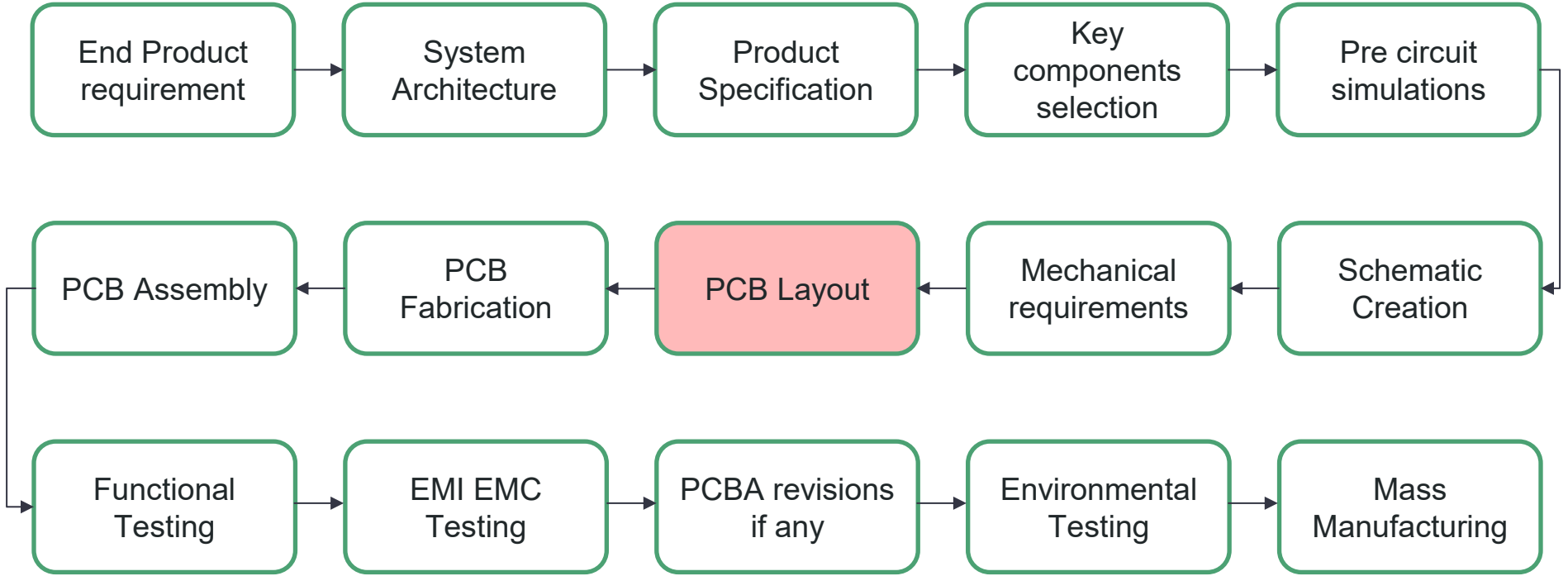
Journey of a Printed Circuit Board (PCB) creation



PCB Design is Multidisciplinary

A well-executed PCB layout bridges the gap between a schematic (theoretical circuit) and a final working product.

Mastering the PCB layout tool is learning to "draw," but without mastering the PCB Design Engineering, one cannot create a flawless PCB.

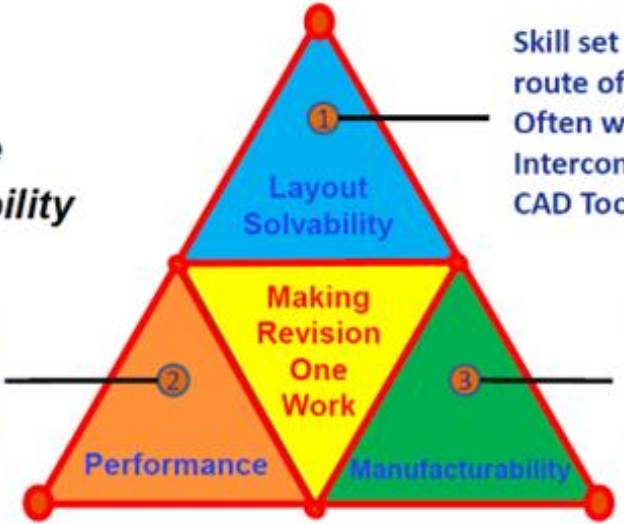
PCB Design engineering encompasses Circuit theory, Electromagnetics, Thermal engineering, Mechanical constraints, Manufacturing processes and Reliability engineering

Printed Circuit Engineering Layout Professional

Today's Circuit Engineer Must Meet 3 Competing Perspectives for Success

Design For:

- DF*Solvability*
- DF*Performance*
- DF*Manufactuability*



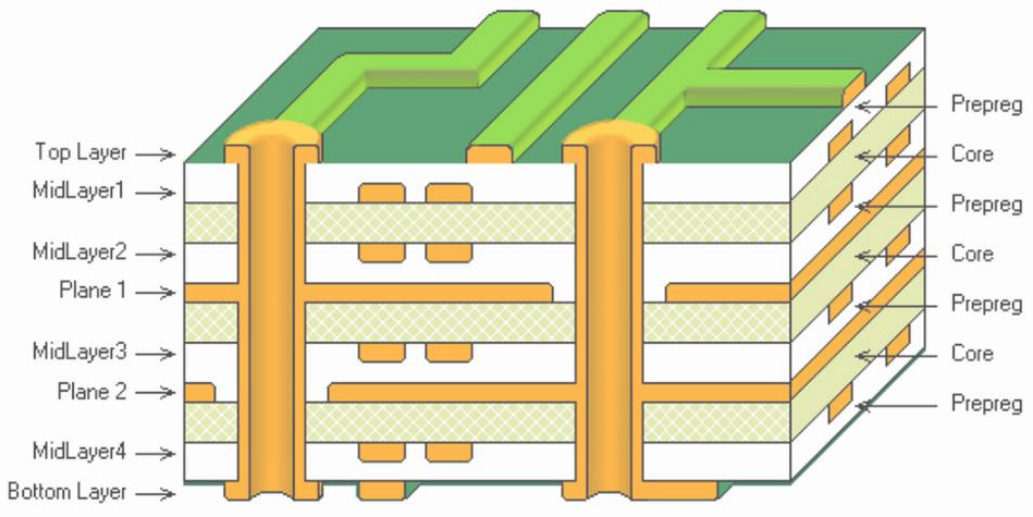
Skill set to solve the placement and route of our circuit.
Often with complex (HDI) High Density Interconnect and master this on your CAD Tool

Signal Integrity/EMC
Power Delivery
Thermal

DFX (DFM) all considerations producing high yield and lower cost

THE RESULT Maximum placement and routing density, optimum electrical performance and efficient, defect-free manufacturing

Courtesy: Siemens



PCB Stack up, PCB measurement units

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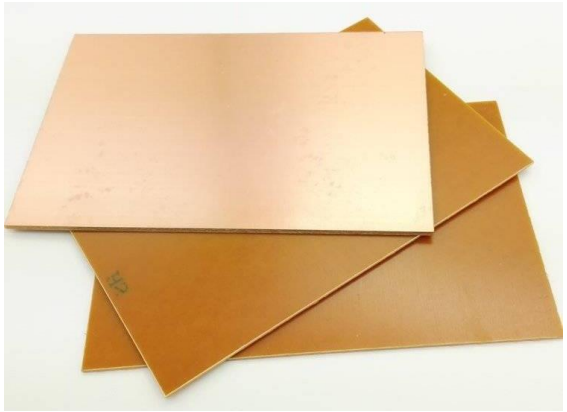
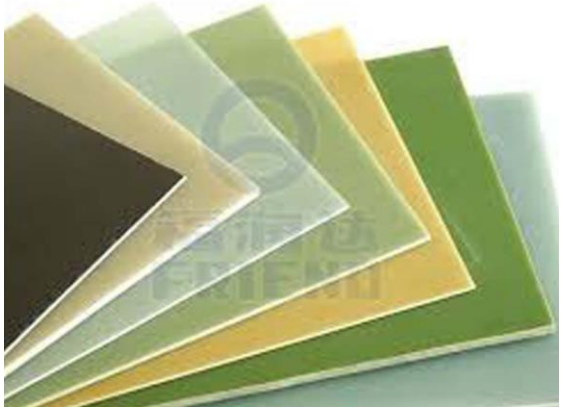
PCB Substrate

The PCB substrate is the "foundation" of the PCB. Selecting the right material depends on Heat tolerance, Max Frequency of operation, and Cost.

Commonly used low-cost PCB substrates for prototype PCBs



Copper Clad, Single side Paper phenolic PCB



Single / Double sided copper FR-1 / FR-4 (**Flame Retardant 4)** PCB

What are common PCB Substrate materials used?

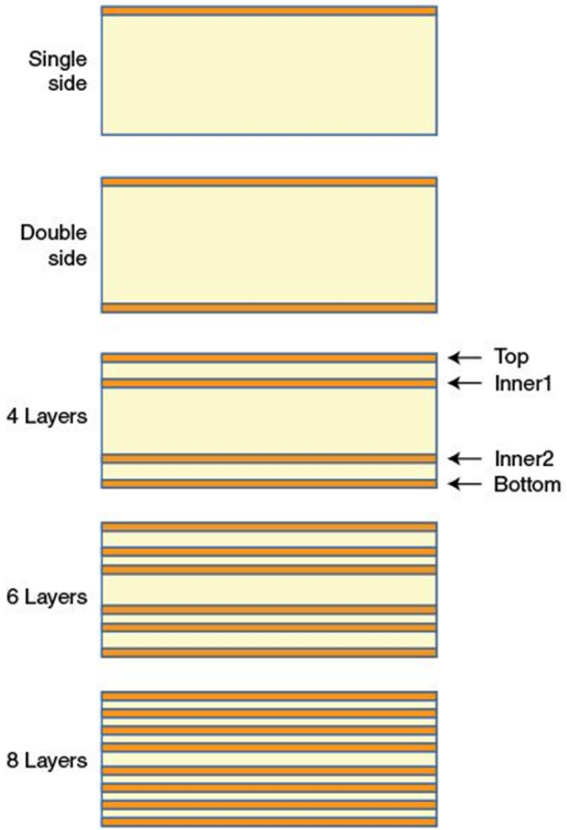
1. **Standard: FR-4 (Flame Retardant 4)**
Composition: Fiberglass cloth embedded in epoxy resin.
Best For: **General-purpose electronics, IoT, and control boards.**
Pros: Low cost, widely available, good mechanical strength.
Cons: Poor performance at high frequencies (>2GHz) and high temperatures.

2. High-Frequency: Teflon (Rogers make)
Composition: Ceramic-filled PTFE (Teflon) or specialized hydrocarbons.
Best For: **RF, Microwave, 5G, and Radar** applications.
Pros: Very low Dielectric Loss (Df); stable Dielectric Constant (Dk) across frequencies.
Cons: Expensive; requires specialized fabrication processes.

3. Thermal Management: Metal Core (MCPCB)
Composition: A copper/aluminum base with a thin dielectric layer.
Best For: **High-power LED lighting**, Automotive headlamps, and Power Converters.
Pros: Incredible heat dissipation (thermal conductivity).
Cons: Limited to single-layer or simple 2-layer designs; heavy.

4. High Temperature: Polyimide
Composition: Advanced polymer resin.
Best For: **Aerospace, Down-hole drilling**, and Flexible PCBs (FPC).
Pros: Handles extreme heat; highly flexible without cracking.
Cons: Higher cost; absorbs moisture more easily than FR-4.

How many Copper Layers a PCB may have?

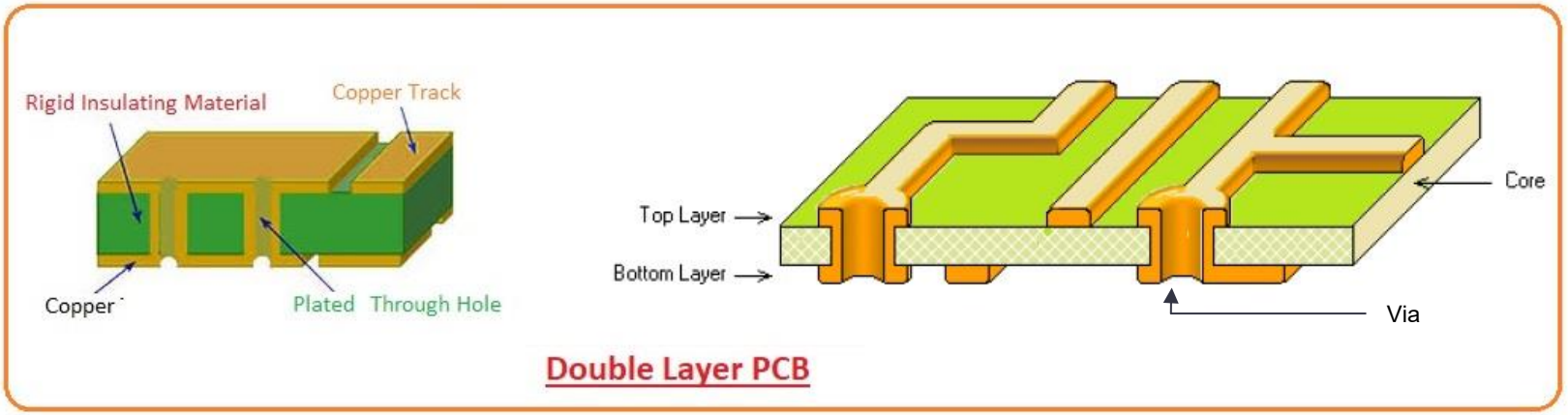


When do we need more than 4 layer PCB?. Multilayer PCBs are necessary when a project requires high circuit density, enhanced signal integrity, compact size, and improved performance that cannot be achieved with single or double-layer boards

How about the cost?
In general cost of the PCB increases as the number of layers. However, it may not be linear and check with the PCB fabricator.

How many copper layers?
Most common – 2 to 32 Layers
High-End Server – 40 to 60 Layers

Two-layer PCB - Example



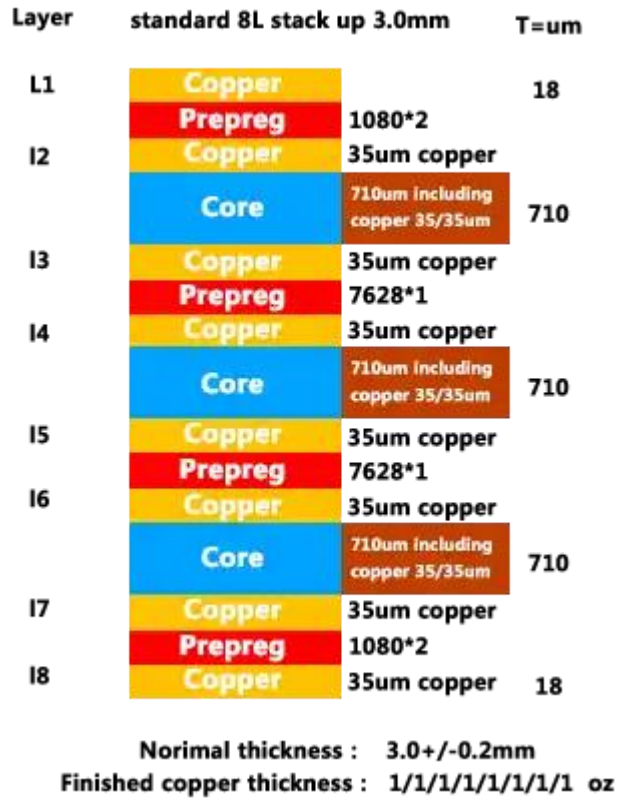
- Centre Insulating Material – FR4 or others
- Top and Bottom layers of FR4 has thin layer of Copper for traces / plane
- Most common for low-cost, less performance critical applications

Standard 2 Layer PCB Stackup for Power PCB

Detailed 8-Layer PCB stack up

Multilayer PCB: Core vs. Prepreg

- **Core:** Fully cured, rigid fiberglass-epoxy laminate with copper foil. Provides structural base and hosts inner circuits.
- **Prepreg:** Semi-cured fiberglass sheet with uncured resin. Acts as adhesive to bond layers during lamination.



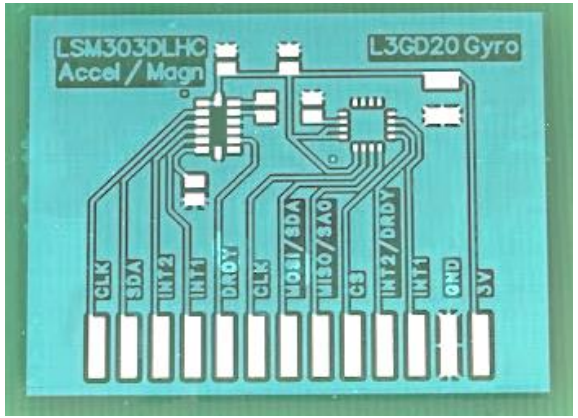
Courtesy: Sierra Circuits https://www.protoexpress.com/blog/best-layout-tips-for-high-speed-and-high-current-pcb-traces/

What is Solder mask?

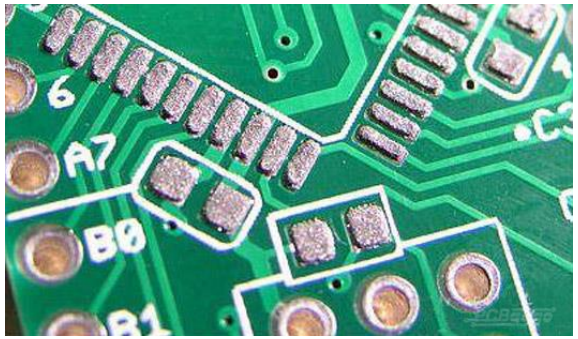
- Solder mask is a thin, protective polymer coating applied to the external copper traces of a printed circuit board (PCB). Here the solder mask is of green color. But other colors are also available.

- **Protection:** Shields copper traces from corrosion, moisture, and contaminants.

- **Solder Control:** Defines areas where solder can flow (e.g., pads for components) and prevents shorts between traces.



Solder mask



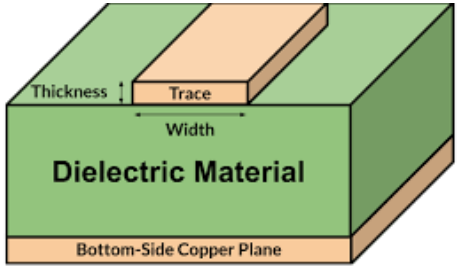
Solder Paste Applied

Courtesy: Sierra Circuits https://www.protoexpress.com/blog/best-layout-tips-for-high-speed-and-high-current-pcb-traces/

What measurement units are used in PCB design?

- PCB measurement units primarily include imperial (mils, inches) for legacy standards, and metric (mm, μm)) for modern design, with special units for material thickness.

- **Trace Width:** Key units used are mils
- 1 mils = 0.001 inch / 0.0254mm
- 1mm = 39.3701 mils



- **Trace thickness:** It is mentioned in micrometers (μm) or ounces (oz/ft^2), mentioned as “oz” for copper weight. A standard 1 oz copper layer is roughly 1.37 mils (35 μm)) thick. A **10-mil trace on 1 oz (1 Ounce)** copper, for instance, is a common reference for carrying **1 amp**.

- **Drill Sizes:** Commonly specified in mils or mm (e.g., 10 mil or 0.25 mm).

How to decide on copper plane thickness?

- **Current requirement:** For Example, 2 oz copper can handle roughly twice the current of standard 1 oz copper for the same trace width without overheating. (IPC 2221 standard covers the amperage calculation for a given trace width)
- **Manufacturing Limits:** Increasing the copper weight typically requires larger minimum trace widths and spacing. For example, **1 oz copper often allows 4 mil spacing, while 3 oz may require 10 mil or more.** So higher thickness will not allow dense trace placement.
- **Thermal Management: Thicker copper acts as a better heat sink**, improving heat dissipation for high-power components like LEDs and MOSFETs.
- **Standard Thickness:** Unless otherwise specified, most fabrication houses will assume 1 oz **(35 μm)** finished copper for your design.

What are the copper thickness used in common?

Copper Weight	Mils	Microns (µm)	Common Application
0.5 oz	~0.7 mils	**17.5 µm**	Inner layers of multilayer boards
1.0 oz	~1.4 mils	**35.0 µm**	Outer Layer for most consumer electronics
2.0 oz	~2.8 mils	**70.0 µm**	Outer layer for Power supplies, high-current circuits
3.0 oz	~4.2 mils	**105.0 µm**	Heavy copper for industrial/automotive

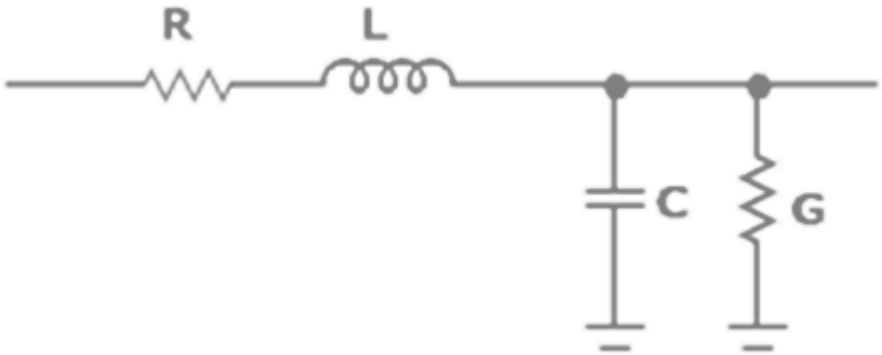
Thicker the copper, higher the current carrying capacity and better is the thermal conductivity.

How to select overall PCB thickness?

Thickness	Typical Use Case
0.2 – 0.4 mm	**Ultra-thin/Flexible:** Wearables, foldable phones, sensors
0.8 – 1.0 mm	**Compact:** Smartphones, tablets, IoT gadgets
1.6 mm	**Industry Standard:** Motherboards, CE, home appliances
2.4 – 3.2 mm	**Heavy-Duty:** Industrial machinery, automotive ECUs

- **Mechanical Stability and Durability:**
  - Thicker boards offer higher rigidity and resistance to bending, warping, or fatigue fractures. Essential for industrial or automotive electronics subjected to vibration.
  - Thinner boards enable wearables and foldable devices.

- **Thermal Management:**
  - Thicker boards have greater thermal mass and can accommodate heavy copper layers (e.g., 2 oz or 3 oz), significantly improving heat dissipation for high-power applications like charging piles or motor controllers.



PCB Physics Fundamentals

CURRENTS, FIELDS, PARASITICS & WHY LAYOUT MATTERS

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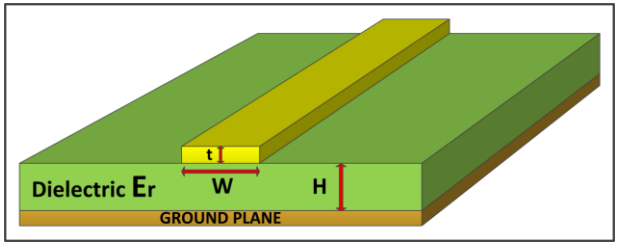
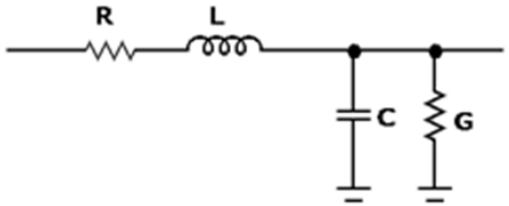
PCB Myths and Realities

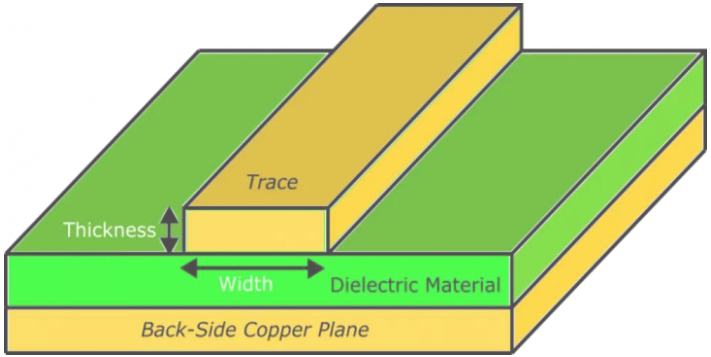
- **PCB trace is assumed to be an ideal wire.**
- **But, the PCB traces have parasitic R**esistance (R), Inductance (L) and capacitance (C).
- Parasitic element's magnitude changes with trace dimensions, and its effects amplified with frequency due to the dependency of L and C with frequency.
- So, for the same schematic, the PCBs done by different engineers can have different performance.



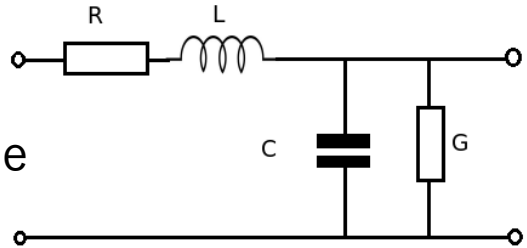


Remember, the Schematic diagram doesn't include the PCB parasitic elements and its values !!!

Electrical Model of a PCB Trace



$$Z_o = \sqrt{\frac{R + jwL}{G + jwC}}$$



Equivalent circuit per unit length

R is resistance of wire/track
L is the inductance
C is the capacitance
G is the conductance of the dielectric

- PCB traces have distributed inductance “L”, capacitance “C” and resistance “R”. G is the conductance of the dielectric between the trace and bottom plane.
- R, L, C and G together determines the impedance Z_0 of the trace. This is important in designs with high-speed signals. **Traces for high-speed interfaces like USB, Ethernet, MIPI and RF etc., needs to maintain a definite, uniform Z_0 of the trace to minimize signal reflections.**

Importance of knowing values of R, L, C and G

- **Inductance** is the most critical factor amongst the parasitic elements.
  - Due to trace inductance, high frequency switching loads such as MCU, MPU, FPGA, and Digital ICs causes **counter-electromotive force (CEMF)** which would disturb the power rails.
  - Magnitude of CEMF is V=-L*(di/dt), where L is the inductance and di/dt is the rate of rise / rate of fall of current. Higher the di/dt (faster rise and fall times), higher will be the CEMF magnitude.

- **Effect of Resistance:** When trace current is high, the trace **resistance "R"** matters. Excessive I^2R loss may cause very high heat, and it may cause the trace burn.

How can we easily estimate PCB parasitic values?

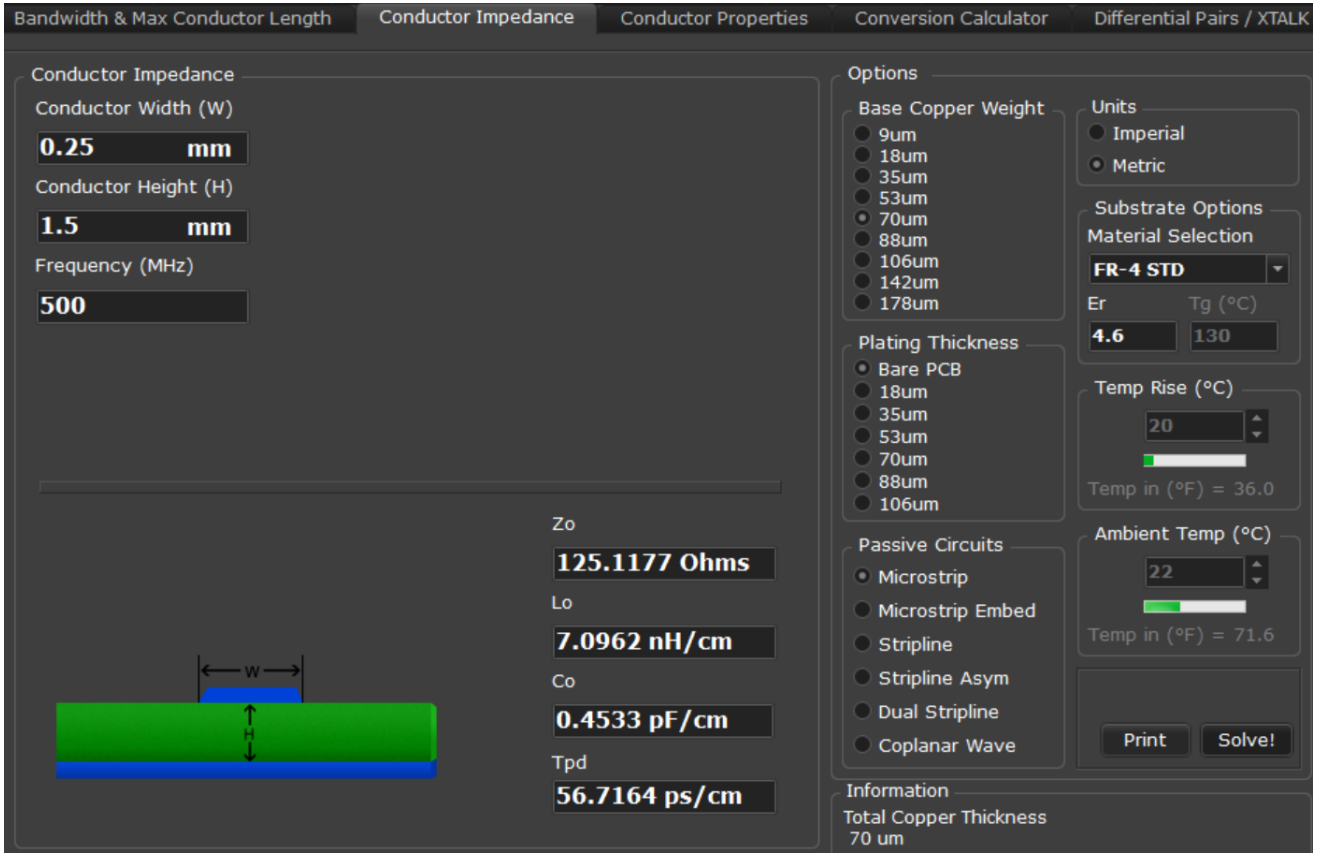
The Saturn PCB Toolkit is a freeware resource for PCB-related calculations !

- Estimates trace resistance, inductance, capacitance
- Evaluates current carrying capacity
- Calculates impedance of PCB traces
- Minimum conductor spacing
- Calculates trace width, gap, height for impedance-controlled traces
- Heatsink design
- Overall helps quantify layout decisions in a quick manner

SATURN PCB DESIGN, INC
Turnkey Electronic Engineering Solutions

Saturn PCB Toolkit - Saturn PCB

L, C of a long wire over a plane



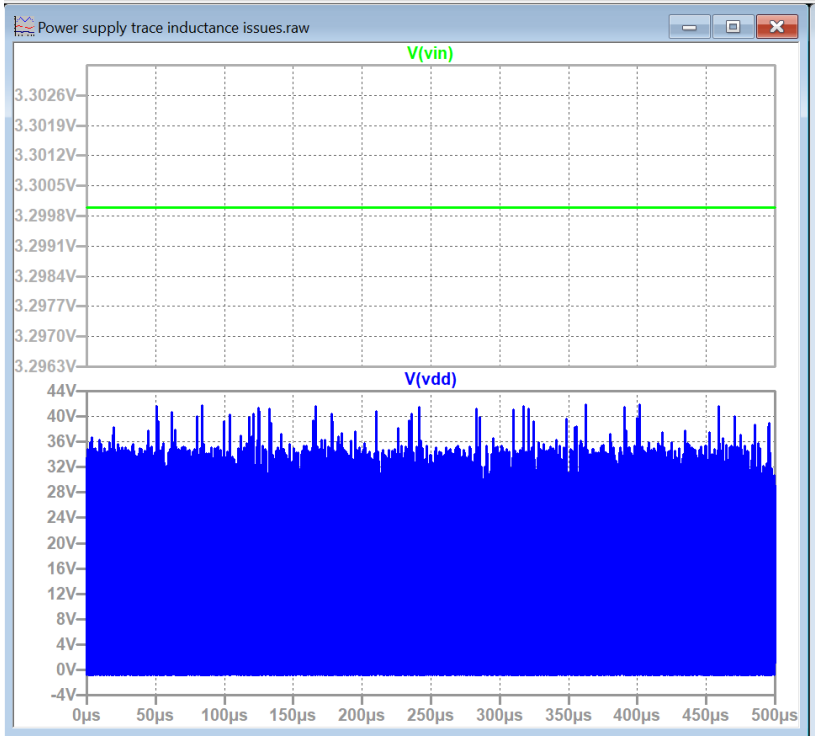
Try changing Conductor width and Height and understand what happens to the Inductance..

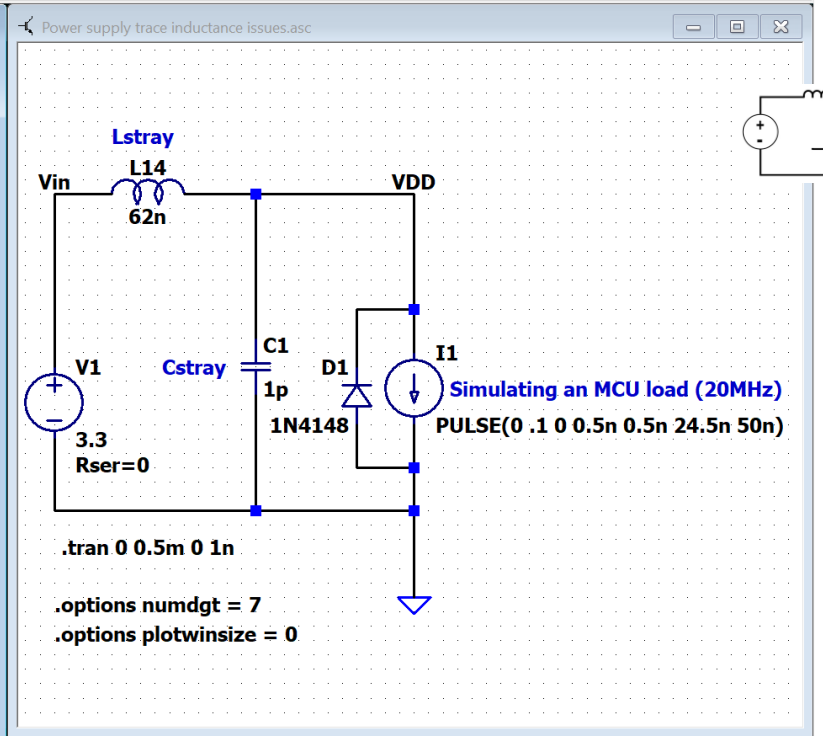
For H = 1.5mm
L = 7.1nH/cm
C=0.42pf/cm

For H = 0.2mm
L = 3.4nH/cm
C=0.94pf/cm

So, what does this convey?

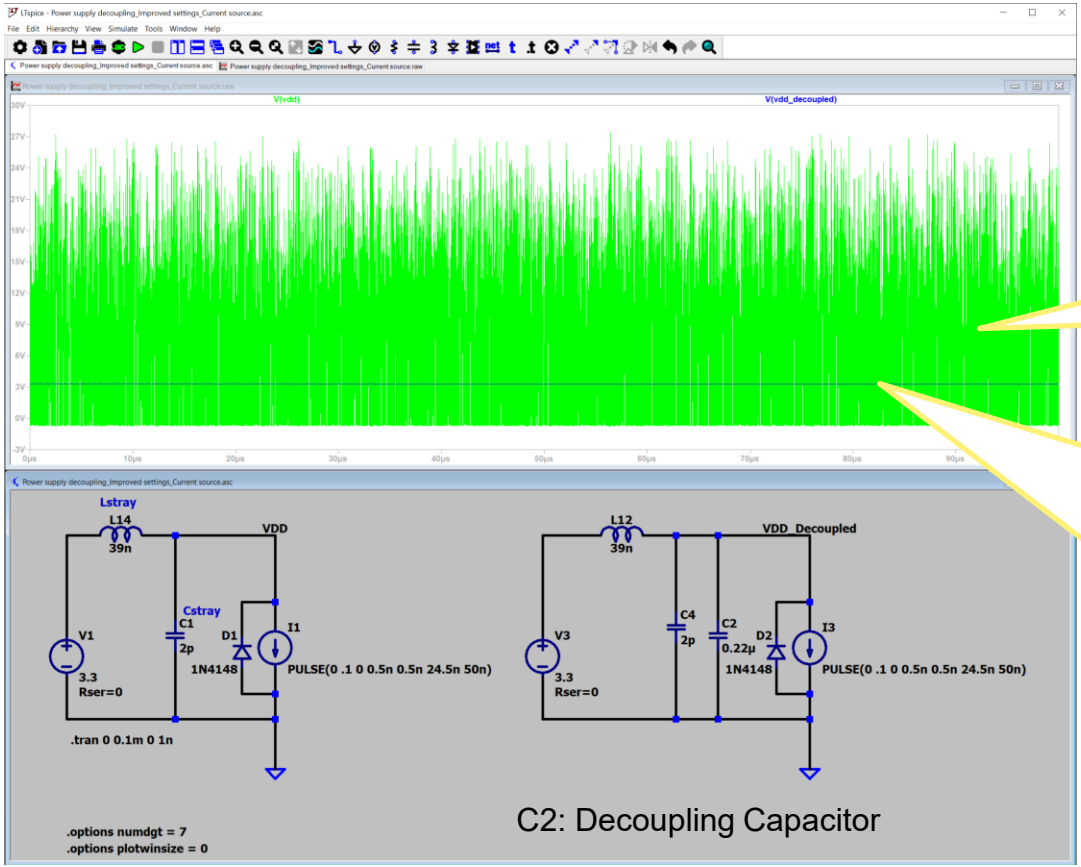
Effect of trace “L” with switching circuits

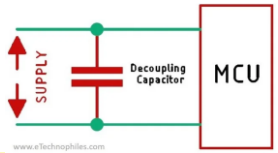




- Trace inductance can be controlled in the PCB layout, but cannot be eliminated, that’s why we need decoupling capacitors for MCU/MPUs

Decoupling V_{DD} : Voltage Waveforms

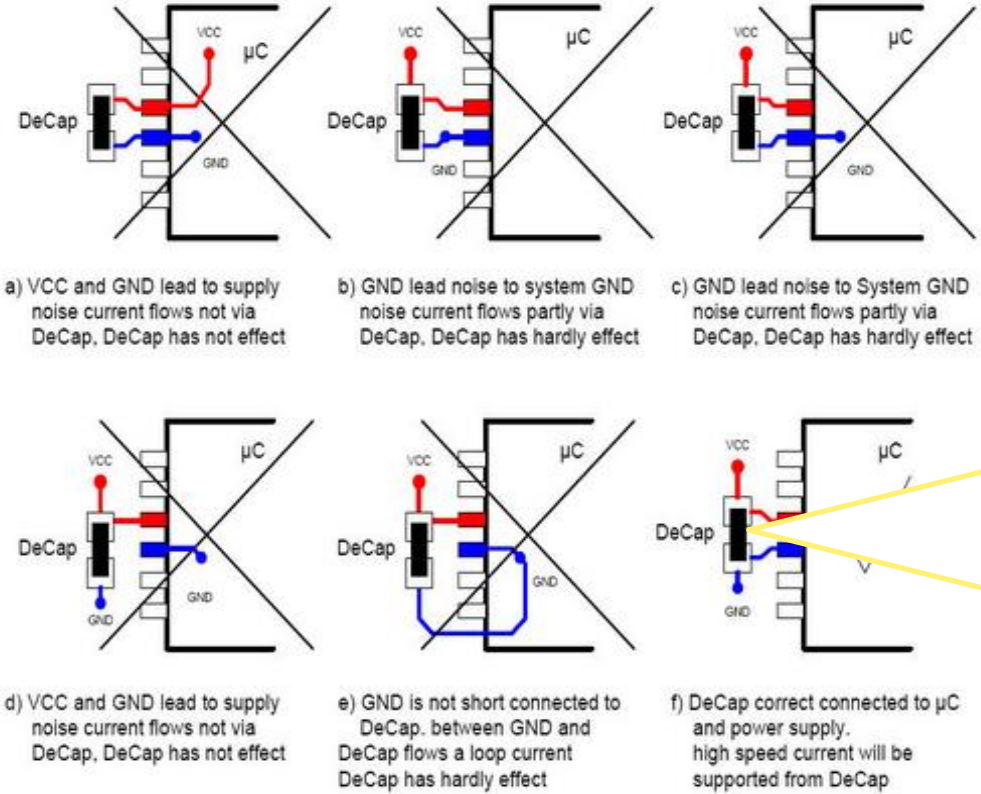




Green Trace: V_{DD} is highly noisy due to the counter emf (L*di/dt) generated by the trace inductance

Blue Trace: Addition of a 0.22uF cap close to the V_{DD} pin eliminates this noise, as the capacitor is able to supply the instantaneous current during switching transients, locally. Thus, decoupling the IC from the effects of trace inductance

Decoupling V_{DD} : Capacitor placement



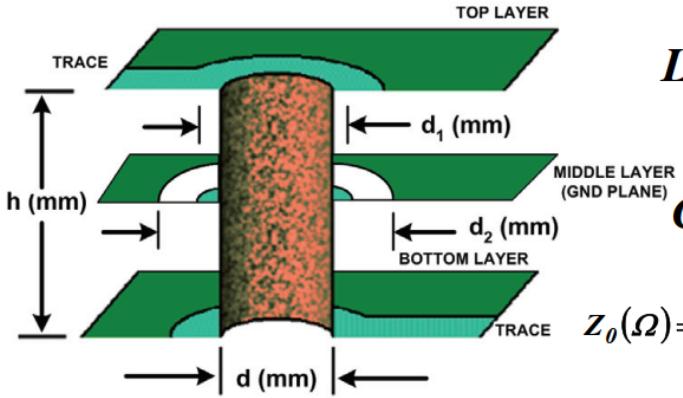
Power supply trace reaches the IC's V_{DD} pin to be decoupled, only after going through the pad of the capacitor. The distance between the IC pin and capacitor pad must be very small (<<50 mils)

Parasitic elements of a Via

Component: Vias

Purpose: Interconnect traces on different layers

Problem: Inductance and Capacitance



$$L(nH) \approx \frac{h}{5}\left[1 + ln\left(\frac{4h}{d}\right)\right]$$

$$C(pF) \approx \frac{0.0555\ \varepsilon_r\ h\ d_1}{d_2 - d_1}$$

$$Z_0(\Omega) = 31.6\sqrt{\frac{L(nH)}{C(pF)}} \qquad T_p(ps/cm) = 31.6\sqrt{L(nH)C(pF)}$$

0.4mm (0.0157”) via with 1.6mm (0.063”) thick PCB has ~ 1.2nH

1.6mm (0.063”) Clearance hole around 0.8mm (0.031”) pad on FR-4 has ~ 0.4pF

e_r = PCB material permeability (FR-4 ~ 4.5)

Courtesy: Texas Instruments

Decoupling V_{DD}: Trace length, Via

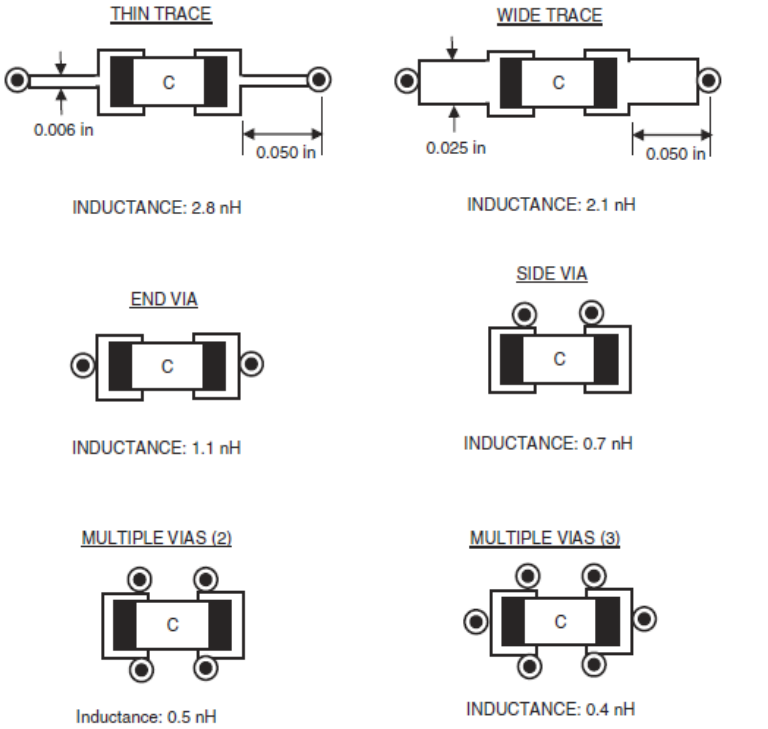
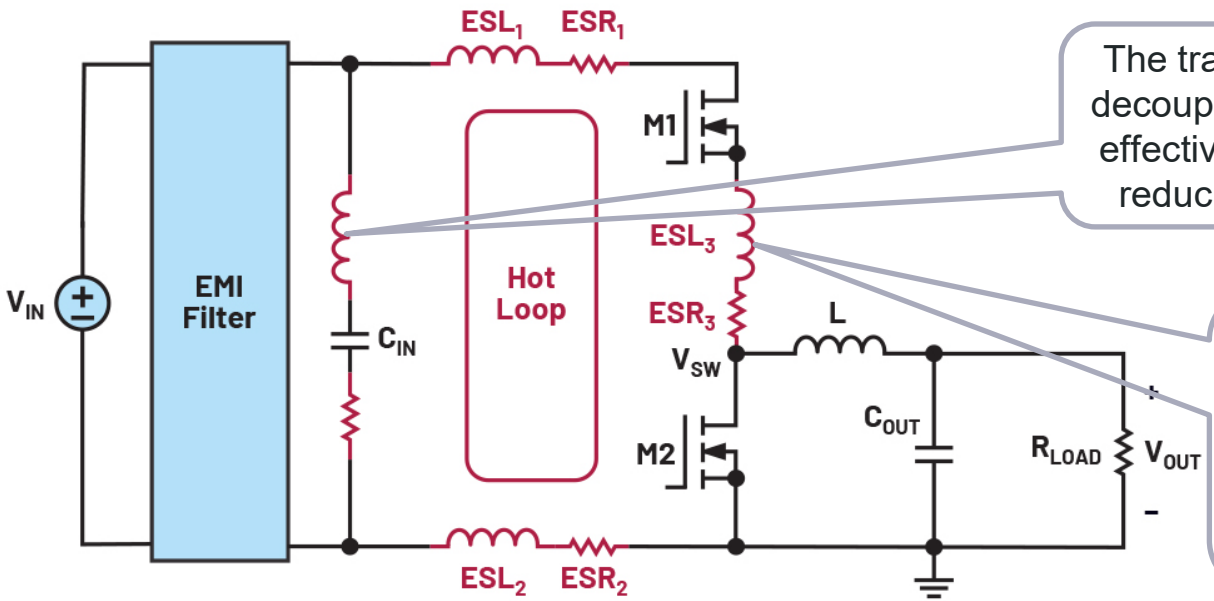


FIGURE 11-25. Inductance of various 0805 SMT decoupling capacitor mounting configurations.

- If via for decoupling capacitor is unavoidable, Then, there are very strict rules on the placement on decoupling capacitor.
- **Rule #1:** The decoupling capacitor must be placed right on the V_{DD} and V_{SS} line of the IC supply to be decoupled. Ideally the connecting trace length should be less than 1 mm.
- **Rule #2:** Ideally, the decoupling capacitor and the IC should be on the same layer. If not, the connecting Vias will add stray inductance and hence placement of Vias and number of vias will be critical.

What is the Effect of trace “L” in Power electronics?



The trace inductance of the bus decoupling capacitor reduces the effectiveness of bus capacitor in reducing the ripple on the bus

The CEMF of the trace connecting MOSFETs could violated the VDS specs of MOSFET, create issues with the gate drive circuit

Due to high magnitude of current and higher switching frequency with fast rise and fall times, the increased trace lengths will have a major impact on the operation of the circuit. Hence the focus needs to be keeping the trace lengths and loop area minimal.

R of a long wire over a plane

Try changing Conductor width and understand what happens to the Resistance..

For W = 0,25mm
R = 0.01440 Ohms/cm

For W = 0,5mm
R = 0.00666 Ohms/cm

So, what does this convey?

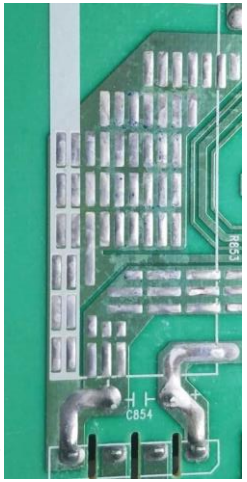
How to find trace width and thickness for a given current

- To calculate the minimum trace width for a high-current track (like 10A), we use the **IPC-2221** curves (historically) or the more modern **IPC-2152** standard. The goal is to ensure the temperature rise (ΔT) due to I^2R heating doesn't exceed a safe limit for the FR-4 material.

- **The Variables**
- Current (I): 10A
- Allowable Temperature Rise (ΔT) : Typically, 10° C to 20° C for industrial applications.
- Copper Thickness: Standard internal layers are usually 1 oz/ft² (35microns), while external layers might be 2 oz/ft² (70microns) for power boards.

Layer Location	Temp Rise (ΔT)	Copper Weight	Required Width
External	10° C	1 oz	~190 mils (4.8 mm)
External	20° C	1 oz	~135 mils (3.4 mm)
Internal	20° C	1 oz	~350 mils (8.9 mm)

Engineering Best Practices for High Current



Even if the math says 3.43 mm width for 10A trace, a professional engineer will apply these industrial "safety nets":

- **The 20% Rule:** Always add a 20% margin to your calculated width to account for manufacturing tolerances in copper etching.
- **Copper Pouring:** Instead of a single trace, use a Copper Region (Polygon Pour) for 10A. This increases surface area and aids in cooling.
- **Via Stitching:** If you must change layers, a single via is not enough. A standard 0.3, mm via can safely handle about 1A to 2A. For 10A, you would need a "Via Farm" of at least 6–8 vias.
- **Solder Mask Opening:** For extreme currents, you can "unmask" the trace (remove the green solder mask) and allow the assembly process to add a layer of solder on top of the copper, effectively increasing its thickness and current capacity.

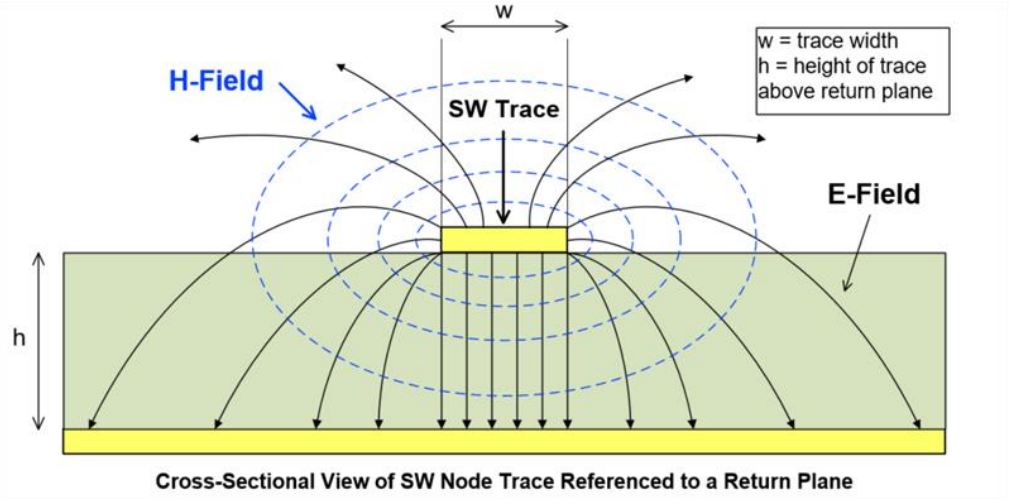
Do you know the components too have parasitic?

- All components, be it Passive like Resistor, Capacitor and Inductors, active semiconductor discretes and ICs have parasitic elements in them.

- Having a clear understanding of these parasitic elements allows you as an engineer to select right components and create products without any design issues. This knowledge improves the product quality and optimizes the design time to the shortest possible.

- You can have a look at these presentations on passive components and it's parasitics to sharpen your product design engineering skillset.

- Passive Components | Seekers Signpost



Electro magnetic fields in a PCB

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Key Concepts and Properties

- **Electromagnetic Fields (EMF):** These are physical fields produced by **stationary charges (electric fields)** and moving charges/**currents (magnetic fields).** They exist around electrical devices, power lines, and natural sources.
- **Electromagnetic Waves:** Created by accelerating charges, these waves propagate through both vacuum and material media. They do not require a medium to travel.
- **Spectrum:** EM waves cover a wide range of frequencies/wavelengths, including radio waves, microwaves, infrared, visible light, ultraviolet, X-rays, and gamma rays.
- **Fundamental Laws:** The behavior of EM fields and waves is described by Maxwell's Equations, which show that a changing magnetic field induces an electric field, and vice versa.

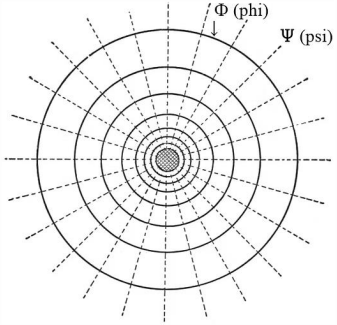
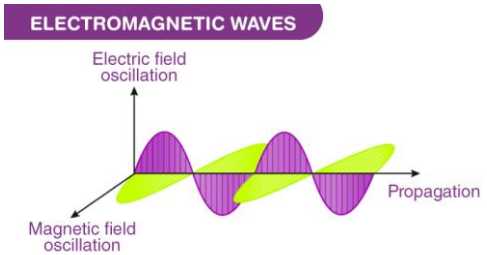
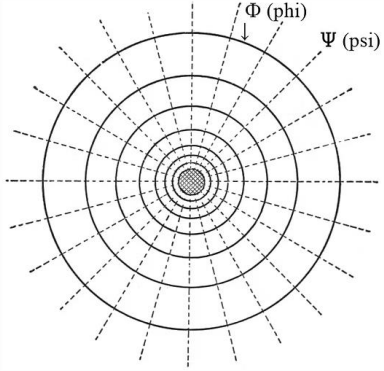


Figure 1 - Electric Field of Conductor.

[Φ magnetic flux; Ψ dielectric flux; from Steinmetz (1911, p.10)]



The role of a Ground plane in a PCB



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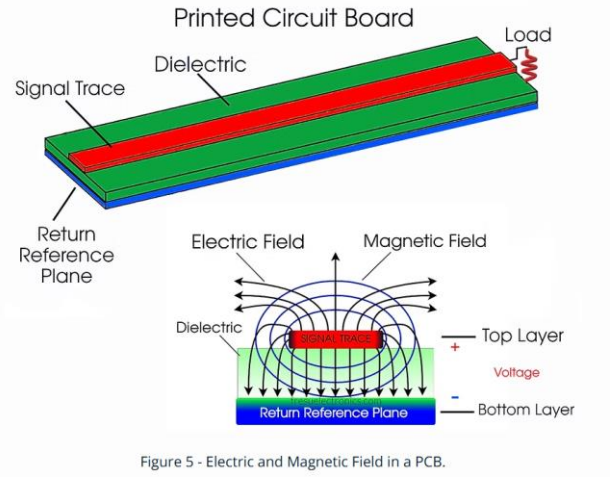


Figure 5 - Electric and Magnetic Field in a PCB.

Assuming a single layer PCB, all traces will have the H fields and E fields associated with it, and nearer the traces are, more the interactions between the traces or the interference. So, single layer PCB is unthinkable for complicated high-density circuits.

Courtesy: fresuelectronics

Amazing benefit of a two or multilayer board is the ability to have a ground plane. With the ground plane, E and H fields of every trace is closely coupled to the ground plane, hence reducing the interference significantly. Still the PCB layout engineer needs to be mindful !

Recap of Electromagnetic Fields

- **Electric fields (E Field)arise from voltage differences or when the voltage in a node or trace changes wildly. Magnetic fields (H Field) come from the current loops.** Together, they form electromagnetic waves that can propagate or couple between elements.
- **Sources:** High-frequency signals (e.g., in RF, digital, or mixed-signal boards), switching power supplies, and external interference (e.g., from nearby devices).
- EM fields are generated by current flowing through traces, vias, components, and power planes.
- **Relevant Physics:** Governed by Maxwell's equations, but in PCBs, we often simplify to transmission line theory (e.g., characteristic impedance, reflections) and near-field/far-field effects.

Challenges associated High speed PCB design

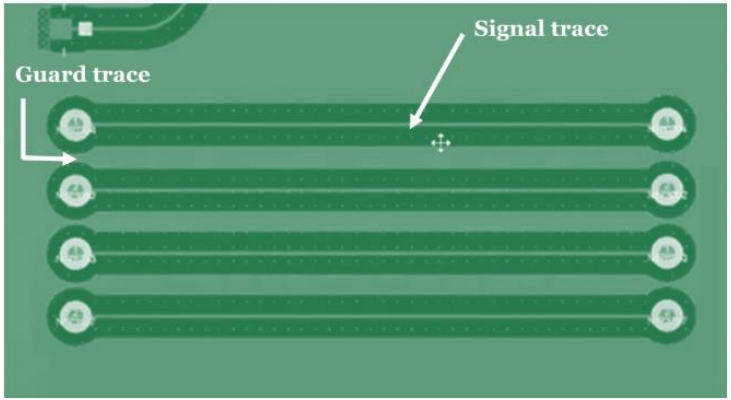
- **Crosstalk:** Coupling of EM fields between adjacent traces or layers, leading to signal distortion. Crosstalk depend on trace spacing, length of coupling, dielectric properties (like those in core/prepreg), and rise times.

- **Signal Integrity Issues:** Reflections from impedance mismatches (due to trace width changes, component pads, Vias etc.,) attenuation in dielectrics, and skin effect (current concentrates on conductor surfaces at high frequencies).

- **Return Paths:** Current always needs a low-impedance return path (e.g., ground plane). Discontinuities like vias or slots can create EM field hotspots, inducing noise.

- **Electromagnetic Interference (EMI):** Unwanted EM fields that disrupt nearby circuits or radiate externally, potentially violating FCC/EMC standards. Common causes: poor grounding, long traces acting as antennas.

Minimizing the interference between nearby traces

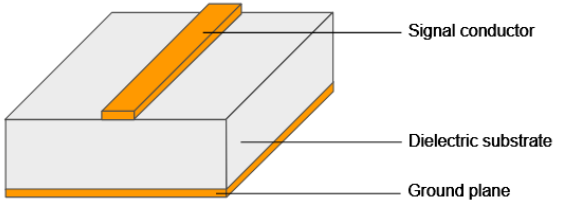


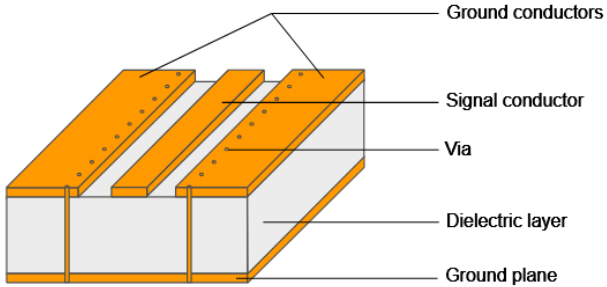
- Place guard traces (Ground) parallel to and surrounding the critical/vulnerable signal traces.
- For best results, connect guards to ground with stitching vias every $\lambda/20$ (where λ is signal wavelength), route them parallel to the signal, and verify with simulations.

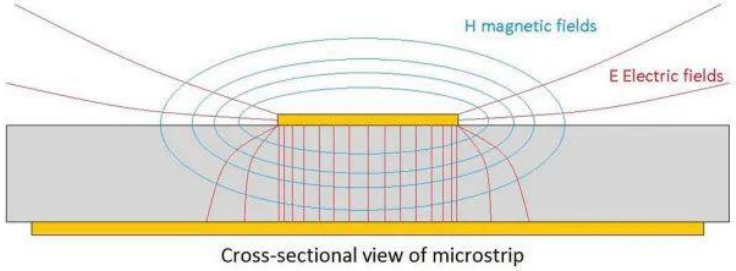
- For low-frequency or non-critical signals, closer spacing of 1W (W-Width of the signal trace) can be acceptable.

- In high-speed designs (>1 GHz), wider spacing like 3W-5W helps preserve characteristic impedance (e.g., 50Ω) by reducing unwanted capacitance from the nearby ground. Always simulate (e.g., using tools like HFSS) for your specific stack up, as rules of thumb can vary by dielectric material and frequency.

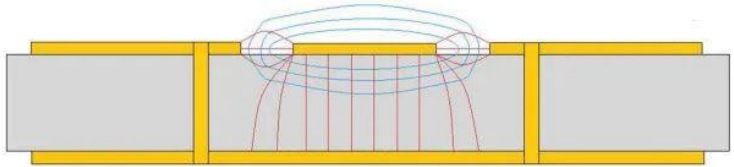
EM Fields: Microstrip Vs GCPW







Cross-sectional view of microstrip



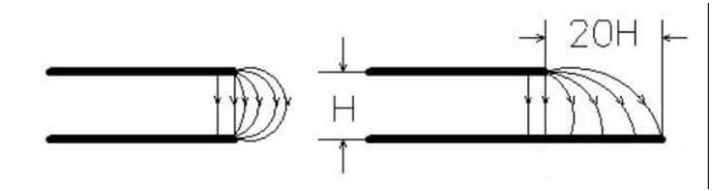
Cross-sectional view of GCPW

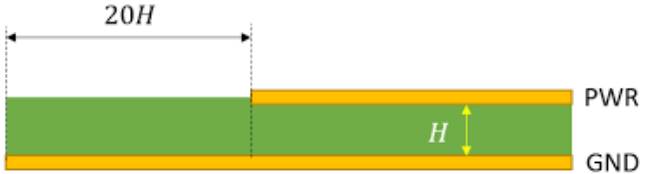
- Structures like Grounded Co-Planar Waveguide (GCPW) ensures that the fields of any RF trace / clock trace is well contained, so that it doesn't interfere with the nearby traces.

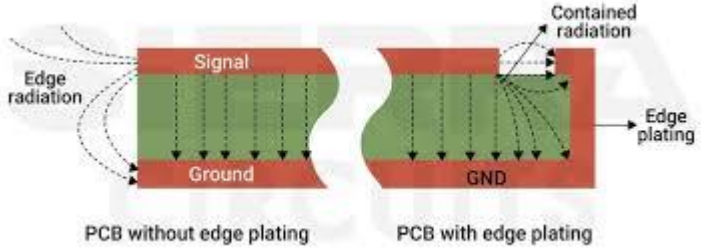
Minimizing the interference between nearby traces

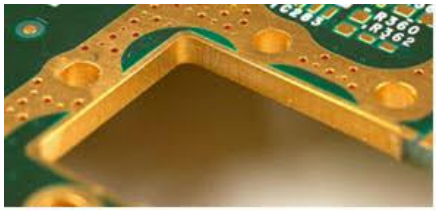
Aspect	Description	Mitigation Techniques
Stackup	Layer arrangement (e.g., signal-ground-signal) influences field containment.	Use continuous ground/power planes; alternate signal layers with reference planes.
Trace Routing	Traces act as transmission lines; fields couple based on geometry.	Minimize length/parallels; use differential pairs; maintain 3W rule (spacing = 3x trace width).
Vias and Holes	Vias can create field discontinuities, leading to stubs or resonances.	Use back-drilling for high-speed; add stitching vias around signals.
Dielectrics	Core/prepreg materials affect field propagation (e.g., lower Dk reduces crosstalk).	Choose low-loss materials (e.g., Rogers for RF); control resin content for uniformity.
Shielding	Contains radiated fields.	Add edge plating, cans, or EMI gaskets; ground enclosures.
Simulation Tools	Predict EM behavior before fabrication.	Use software like HFSS, SIwave, or HyperLynx for field modeling and analysis.

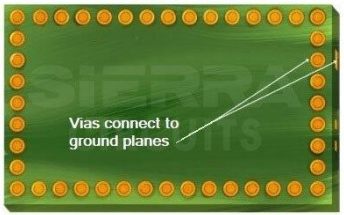
Controlling fringing flux at the PCB edge



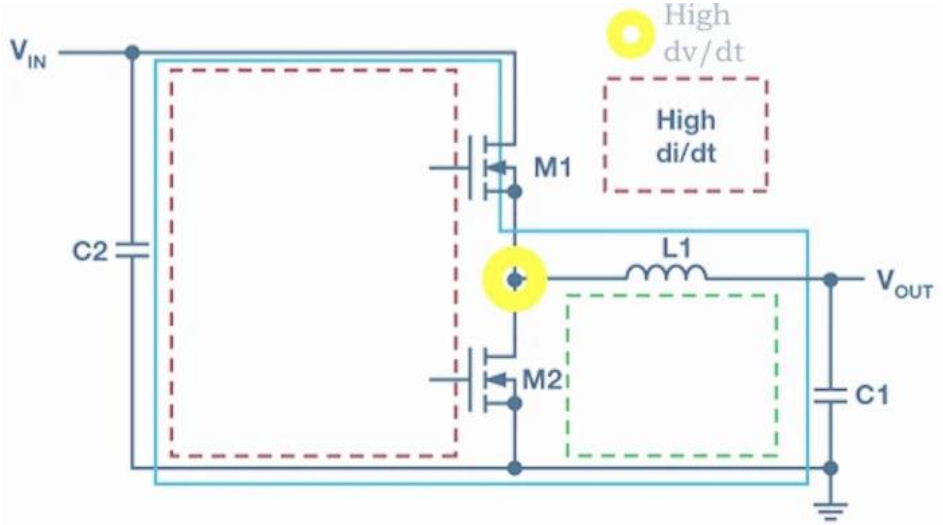








- Assume the edge of the PCB is close to a metal casing or another PCB and in this case if the supply traces or plane goes all the way to the edge, then the fringing flux could cause interference.
- Few ways of mitigating this are 1) use 20H rule, that is keeping the positive traces or plane away from the edge by 20H distance 2) plate the edge with ground plane 3) Use via fencing at the edge of the PCB to connect stitch the ground planes



Loop area in PCB

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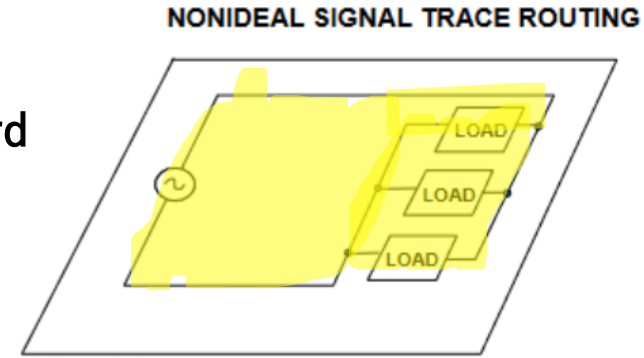
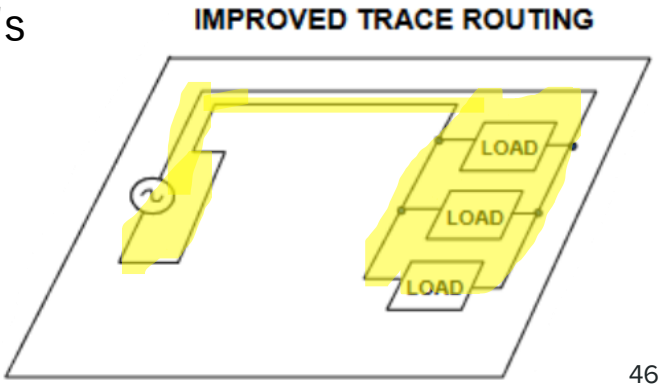
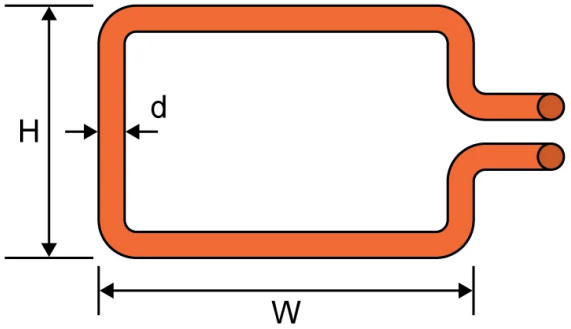
Understanding Loop Area in PCB Layout

- In PCB design, the "loop area" refers to the physical **area enclosed by a current-carrying trace (the forward path) and its return path** (typically ground or power return).
- Every signal or power current forms a closed loop, and the size of this loop directly impacts the board's electromagnetic behavior.
- Minimizing loop area is a fundamental principle in high-speed, high-power, or EMI-sensitive designs.





Rectangle Loop Inductance Calculator



Diameter of wire : 0.1mm Number of turns : 1 Relative Permeability: 4.2	
W, H	Inductance
5 mm	64 nH
10 mm	152 nH
20 mm	351 nH

Equations

$$L_{rec} = \frac{\mu_o \mu_r}{\pi}\left[-2\,(W+H) + 2\sqrt{H^2+W^2} - H\ln\left(\frac{H+\sqrt{H^2+W^2}}{W}\right) - W\ln\left(\frac{W+\sqrt{H^2+W^2}}{H}\right) + H\ln\left(\frac{2H}{\frac{d}{2}}\right) + W\ln\left(\frac{2W}{\frac{d}{2}}\right)\right]$$

W = width of the loop

H = height of the loop

d = diameter of the wire

μ_r = relative permeability

μ_0 = permeability of free space = 4π x 10-7

Smaller the area of the loop(H x W), smaller the loop inductance, lesser the radiation

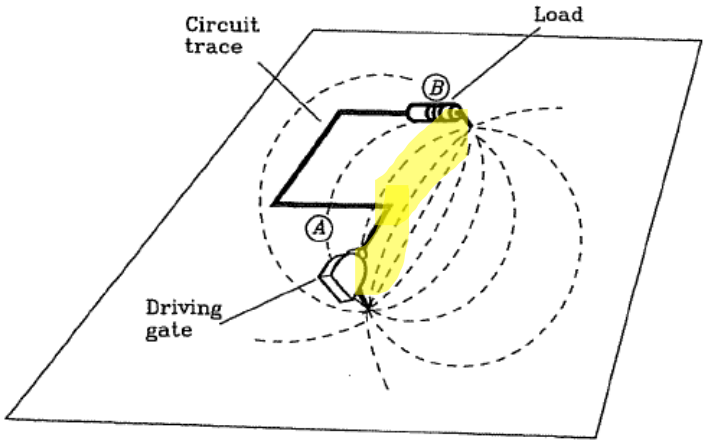
Courtesy: Rectangle Loop Inductance Calculator - Engineering Calculators & Tools

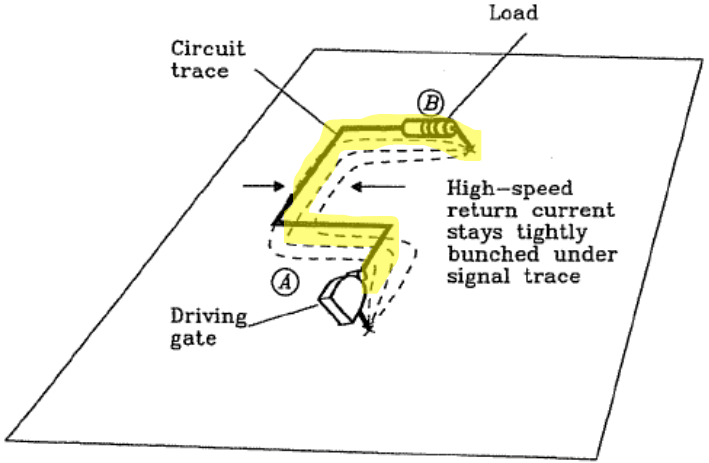
Why loop area matters

- **Inductance: Larger loops increase parasitic inductance (L),** calculated roughly as **L ≈ μ_0 * (loop area / length),** where μ_0 is the permeability of free space.
- High inductance causes voltage spikes **(V = L * di/dt)** during fast switching, leading to ringing, overshoot, or signal distortion in digital circuits.
- **EMI Radiation:** A large loop acts like an antenna, radiating electromagnetic fields proportional to the loop area and current frequency.
- **Susceptibility to Interference: Bigger loops are more prone to picking up external magnetic fields and also radiate** (via Faraday's law: induced EMF = -dΦ/dt, where Φ is magnetic flux through the loop), resulting in crosstalk or noise injection from nearby traces or sources.

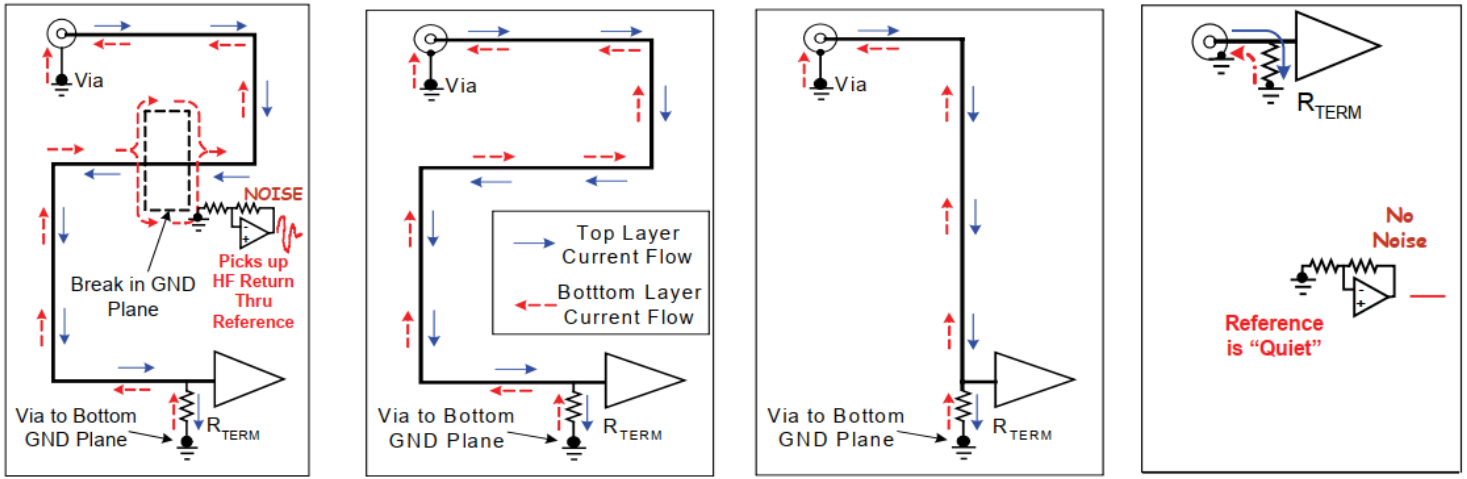
Ground plane and return current path

- Ground planes serve several functions. 1) Return path for signal current, 2) stable voltage reference
- DC current flows along path of least resistance.
- For AC (f > 0) current follows the path of least impedance. Inductance compels the return path current to flow beneath the signal trace (proximity effect)





Always think of minimizing the loop area



WORST

Large Current Loop + Discontinuous GND Plane

BAD

Large Current Loop

BETTER

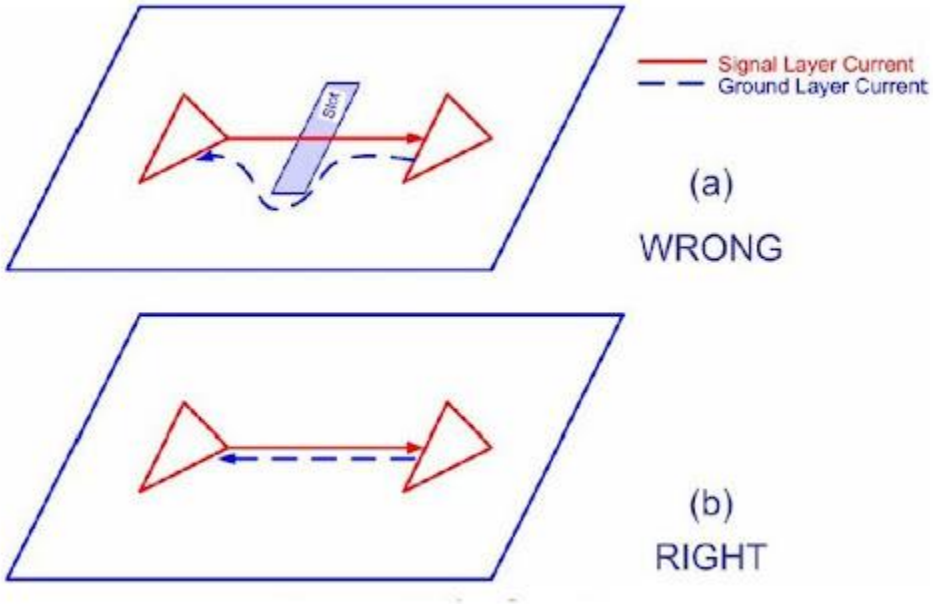
Reduced Current Loop

BEST

Minimum Current Loop

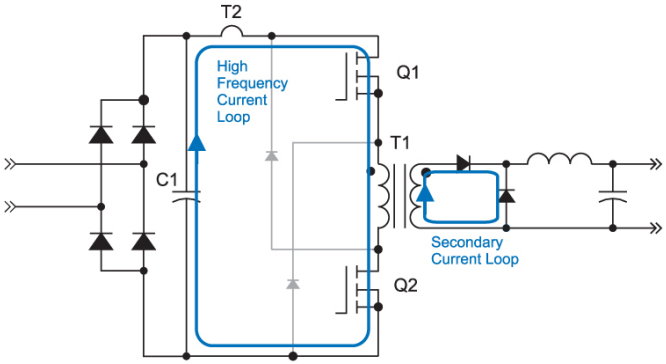
Courtesy: Texas Instruments

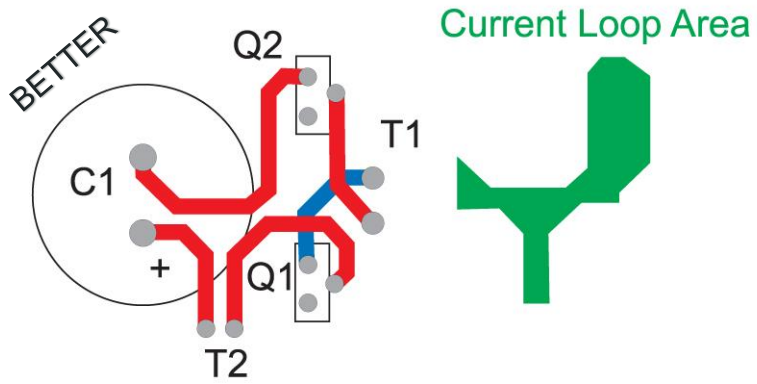
Interrupted return path increases loop area

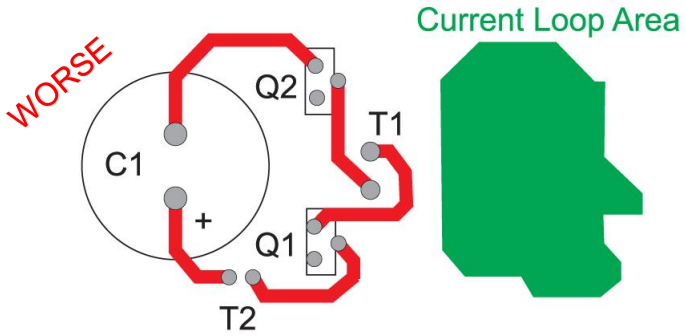


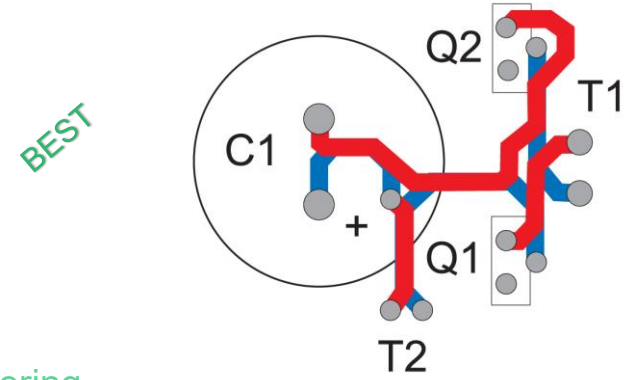
- Uninterrupted ground plane is needed for both single ended signals to ensure shortest return path and hence shortest possible loop area
- Uninterrupted ground reference plane is even more critical for impedance-controlled lines to have a controlled uniform impedance

Components placement to reduce loop area



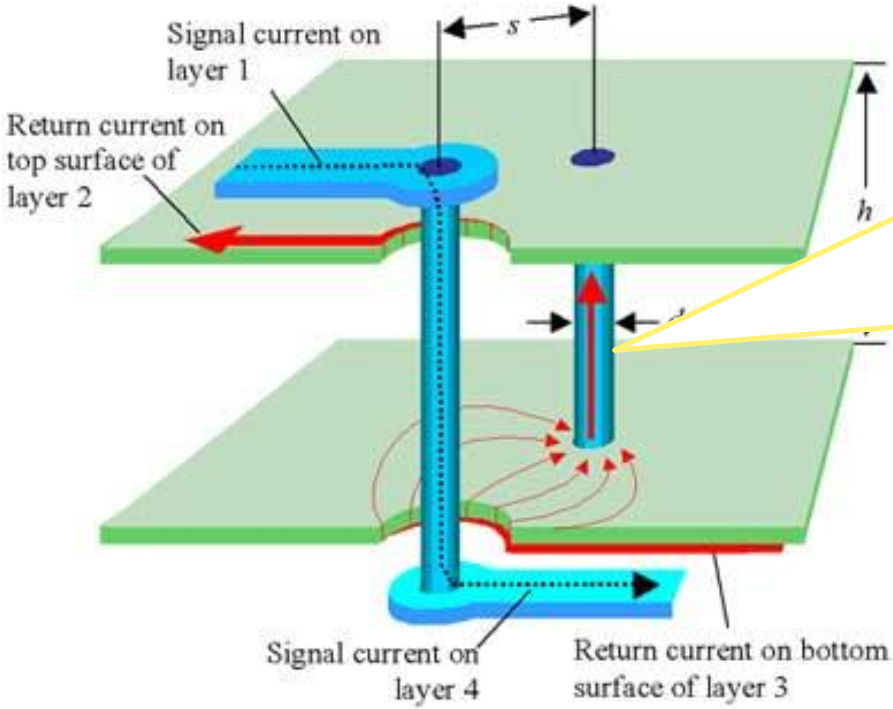






Courtesy: RIDLEY Engineering

Ensure Ground return paths when switching layers



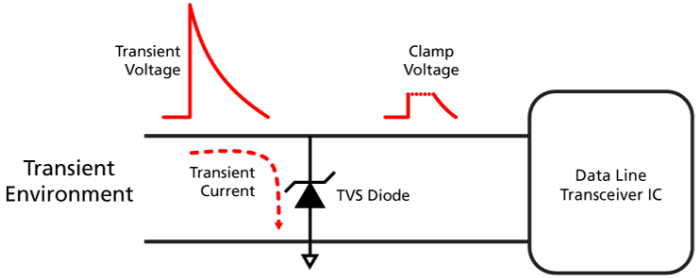
In a multi layer PCB, when a signal trace switches from one layer to another, there needs to be closest ground return path next to the via. This can be accomplished by placing one or two vias close the signal trace via

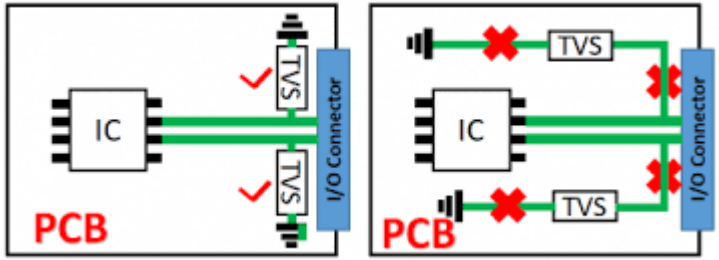
Courtesy: Signal Consulting Inc Short-Term Impedance of Planes

Strategies to minimize loop area

- **Use Ground Planes:** Route signals over continuous ground planes—**the return current follows the path of least impedance directly beneath the trace, minimizing the loop.**
- **Avoid Splits/Slots:** Don't cut the ground planes unnecessarily, as this forces return currents to detour, enlarging loops.
- **Short, Direct Paths:** Keep components close; avoid long detours for returns. For differential pairs, route them tightly together.
- **Ground Vias and Stitching:** Use ground vias to connect all ground layers, preventing loops from spanning multiple planes.

ESD Protection components placement





- Any connectors on a PCB can be a source of ESD discharge through human contact and failure of ICs.
- Hence ESD diodes / TVS diodes are used very close to each pin of the connector to safely redirect the ESD discharge current away from the IC being protected.
- The routing trace length for the ESD diodes needs to be thick and very short in length to minimize the parasitic inductance of the connecting trace

Keep the current loop from connector pin to ESD and the Ground, the smallest. Use thickest possible trace.

Switching regulator layout example

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Typical schematic of an EMI optimized buck converter

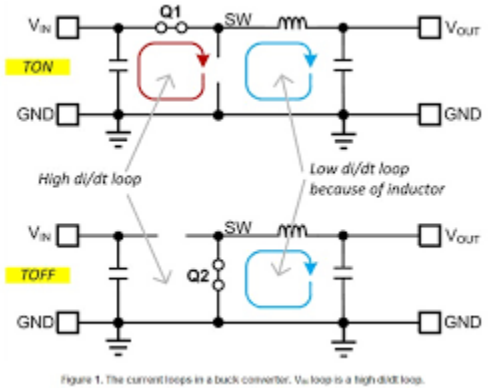
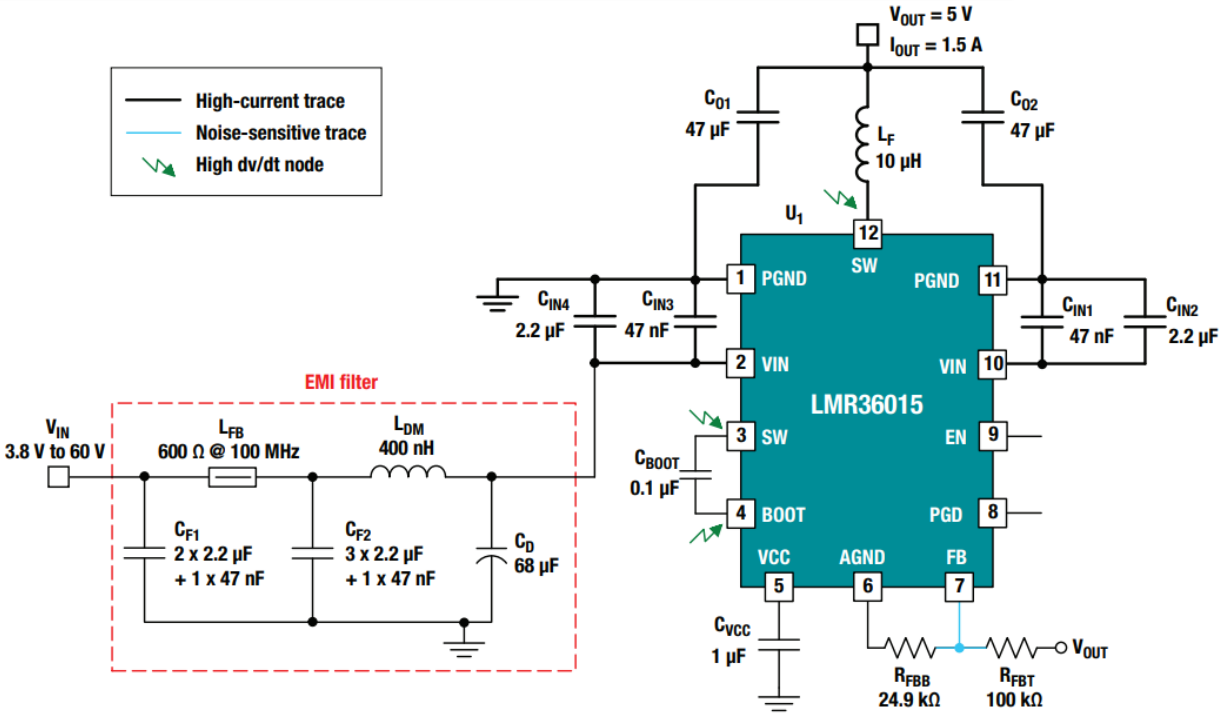


Figure 1. The current loops in a buck converter. V_{IN} loop is a high di/dt loop.

Two critical loops in a Buck Regulator



DC/DC converter with EMI-optimized package and pinout. Included is a two-stage EMI input filter.

Courtesy: [An Engineer's Guide to Low EMI in DC/DC Regulators: Texas Instruments]

Buck Regulator Layout challenges

- **1. The "Hot Loop" (The #1 Priority):**The path consisting of the Input Capacitor (C_IN), High-Side MOSFET, and Low-Side MOSFET (or Diode) carries discontinuous, high di/dt current.
  - ***The Challenge:*** Minimizing the area of this loop to prevent EMI and voltage ringing.
  - ***The Fix:*** Place C_IN as close as possible to the MOSFET pin / Vin pin of the regulator.
- **2. The Switch Node (SW):**The node connecting the MOSFETs and the Inductor. It has high dV/dt (fast voltage swings).
  - ***The Challenge:*** It acts as an antenna, radiating noise to nearby sensitive signals.
  - ***The Fix:*** Keep the trace short and wide; void the ground plane directly underneath to reduce parasitic capacitance.
- **3. Feedback (FB) Routing:** The sensitive analog signal that tells the IC to adjust the voltage.
  - ***The Challenge:*** Picking up noise from the Inductor or Switch Node.
  - ***The Fix:*** Route the FB trace away from the SW node; use a "Kelvin Connection" at the output capacitor.

Power stage PCB routing to reduce EMI

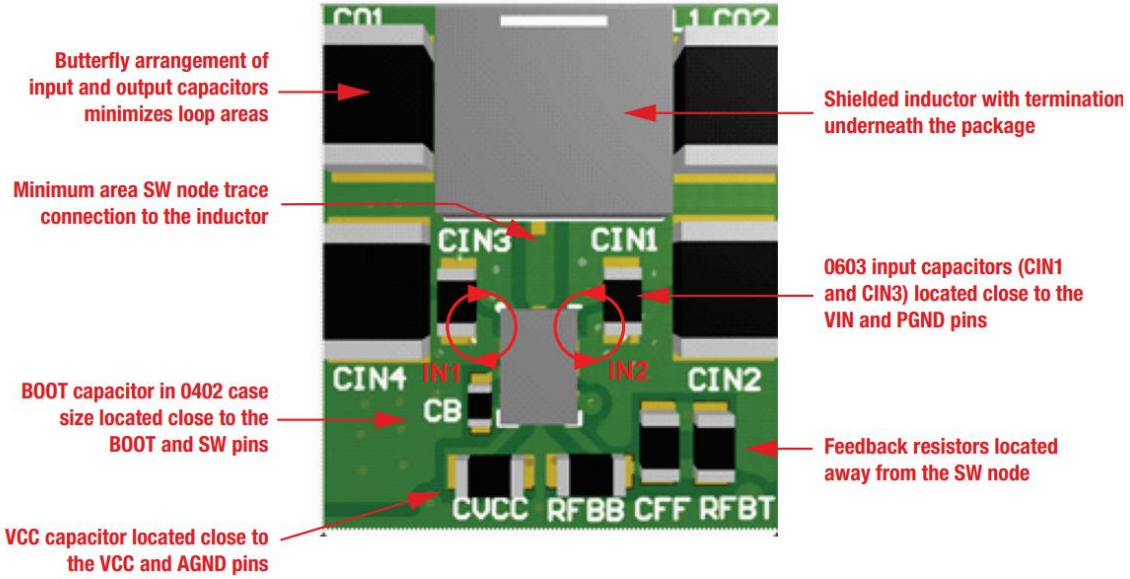


Figure 7. Power-stage layout routed only on the top layer of the PCB.

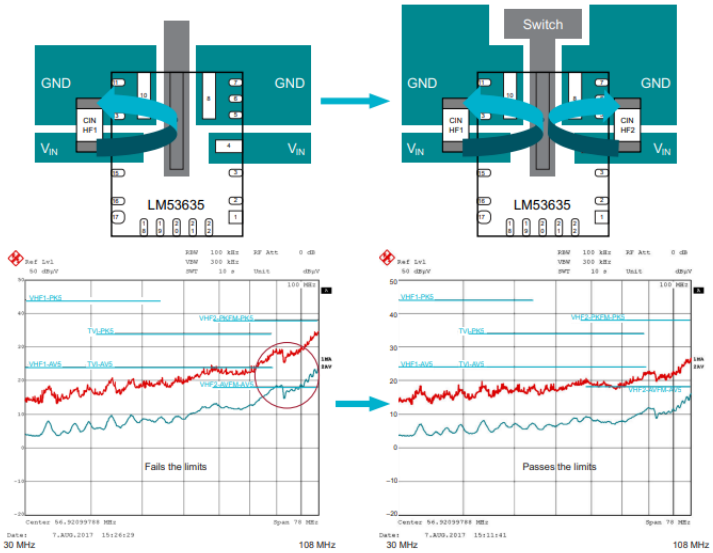


***Figure 18.** Effect of the parallel input path on EMI in an SMPS.*

Courtesy: Time-Saving and Cost-Effective Innovations for EMI Reduction (Rev. A): Texas Instruments

Courtesy: An Engineer's Guide to Low EMI in DC/DC Regulators: Texas Instruments

PCB Layout enabled by pinout of the converter

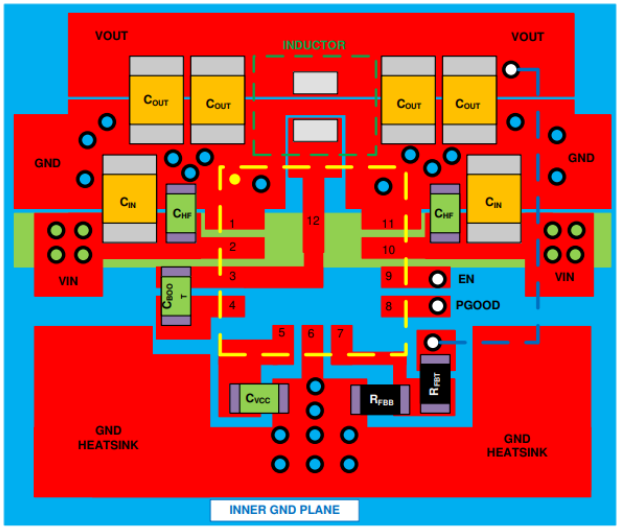


Figure 12-2. Example Layout

- Position input capacitors close to VIN and GND pins, which are adjacent.
- Place the VCC bypass capacitor near the VCC pin with short, wide traces.
- Locate the CBOOT capacitor close to the device using wide, short traces to BOOT and SW pins.
- Keep the feedback divider components close to the FB pin with short connections; avoid routing near noise sources.
- Use at least one ground plane in a middle layer for noise shielding and heat dissipation.
- Ensure wide, direct paths for VIN, VOUT, and GND to reduce voltage drops and improve efficiency.
- Allocate sufficient PCB copper area for heat sinking, using at least one-ounce copper layers and thermal vias if multilayered.
- Minimize the switch area by keeping the SW-to-inductor copper short and wide, reducing EMI.

Courtesy: LMR36015S 4.2-V to 60-V, 1.5-A Buck Converter

IC Pinout and packaging optimizations for low EMI

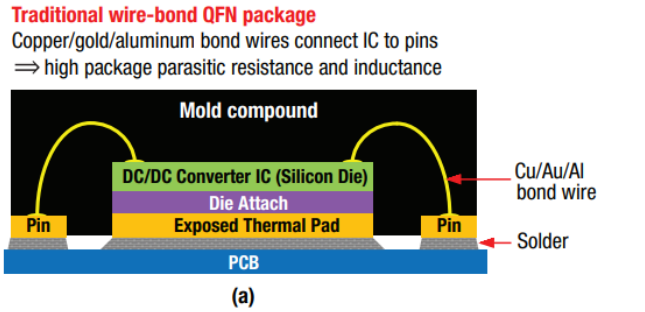
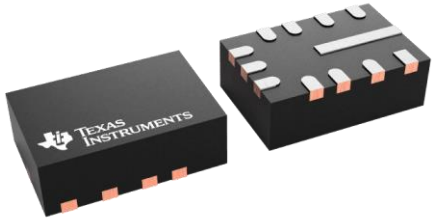


Figure 8. *Wire-bond QFN (a) and HotRod FCOL (b) package construction comparison.*

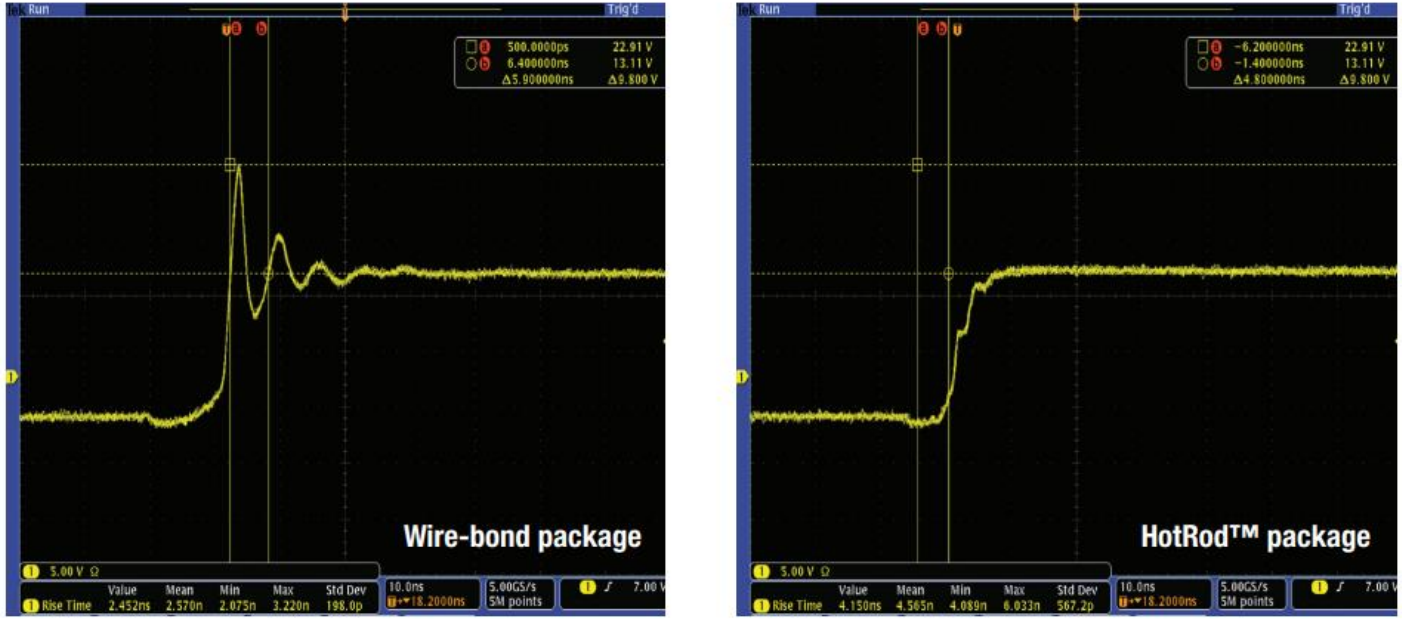


From an EMI standpoint, the HotRod package lowers package parasitic inductance versus traditional wire-bond packages.

HotRod package result in much lower ringing at the switching commutations (a 50 MHz to 200 MHz frequency range)

Courtesy: An Engineer's Guide to Low EMI in DC/DC Regulators: Texas Instruments

Switch node waveform comparison



Switch-node voltage waveform with a traditional wire-bond converter (a); and a HotRod FCOL converter (b).

Courtesy: An Engineer's Guide to Low EMI in DC/DC Regulators: Texas Instruments

High Speed PCB Layout Design Fundamentals

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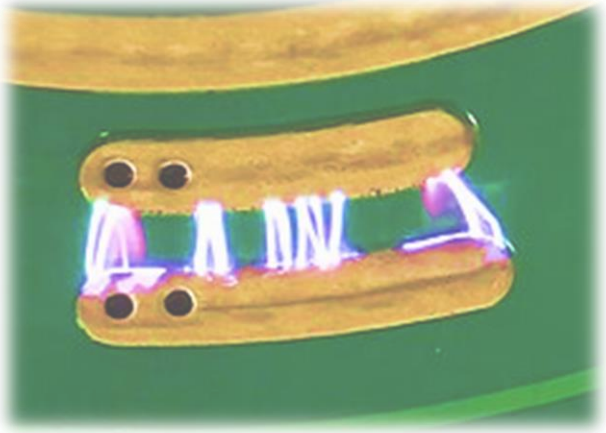
High Speed PCB Design – Reference Materials

There are comprehensive materials available on the internet on this topic. Below are a few curated ones to go through.

- High Speed PCB Design – Sierra Circuits
- Impedance for Everyone – WURTH ELECKTRONIK
- High Speed Signal Integrity Principles
- Toradex – High speed PCB Layout design guide
- Texas Instruments - High-Speed Interface Layout Guidelines
- Charles Pfeil -High-Speed Constraint Values and PCB Layout Methods
- Infineon - EMC and System-ESD Design Guidelines for Board Layout



Minimum Conductor spacing

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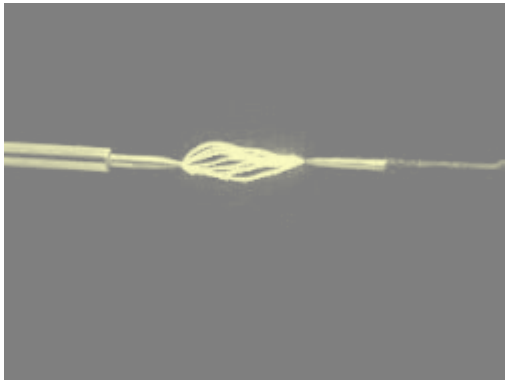
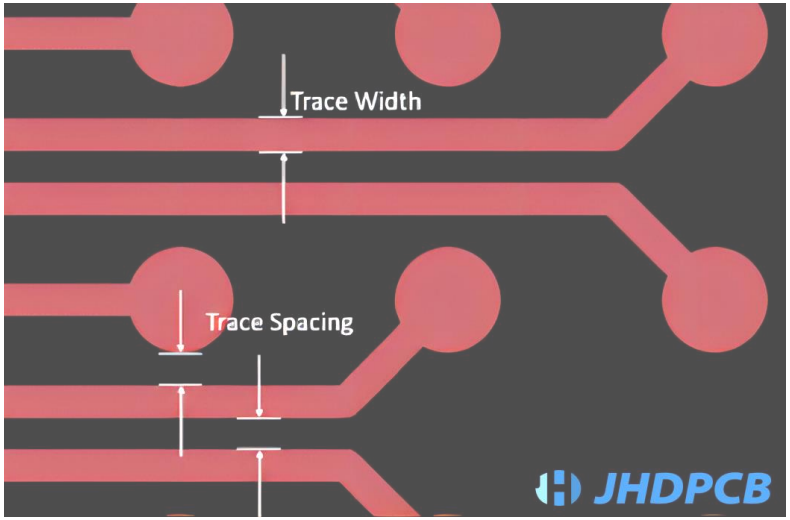
Introduction to trace spacing

- Proper distances between PCB traces are critical to avoid flashover or tracking between electrical conductors.



When the voltage across two exposed conductors exceeds a threshold, an arc occurs



PCB Trace Minimum Spacing Requirements

- **Trace Spacing Requirements:** Minimum distances between conductive elements (traces, pads, vias) to prevent arcing, shorts, crosstalk, and ensure safety/reliability. **Influenced by voltage, environment, and board type.**
- **Key Factors:** Voltage (DC/AC peak), altitude, coatings (e.g., solder mask), pollution degree, and manufacturing tolerances.
- **IPC Standards:** Provide guidelines for clearance (through air) and creepage (along surface). Main standard: **IPC-2221** (Generic Standard for Printed Board Design).
- **IEC Standards:** Standards such as **IEC 60335-1** cover the safety requirement in much more detail. For a product development, one must comply this too.
- **Importance:** Ensures electrical safety, signal integrity, and compliance

Trace spacing concepts

- **Clearance:** Shortest path through air—prevents flashover/arcing. (This is specified in IPC 2221 standard)
- **Creepage:** Shortest path along insulating surface prevents tracking due to contamination/moisture. (Creepage distances are often larger than clearance due to the risk of surface tracking. This the designer needs to ensure)
- **3W Rule:** Spacing ≥ 3x trace width for crosstalk reduction (not IPC-mandated, but common for signal integrity).

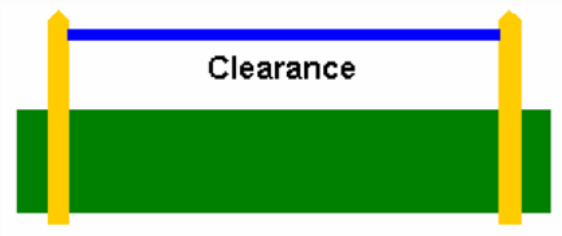


Figure 1: Clearance (In Air)

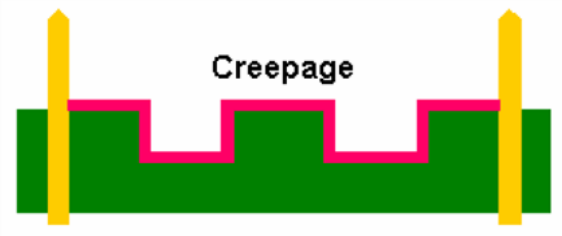


Figure 2: Creepage (Along Surface)

Courtesy: Optimumdesign.com

Electrical conductor spacing – IPC2221

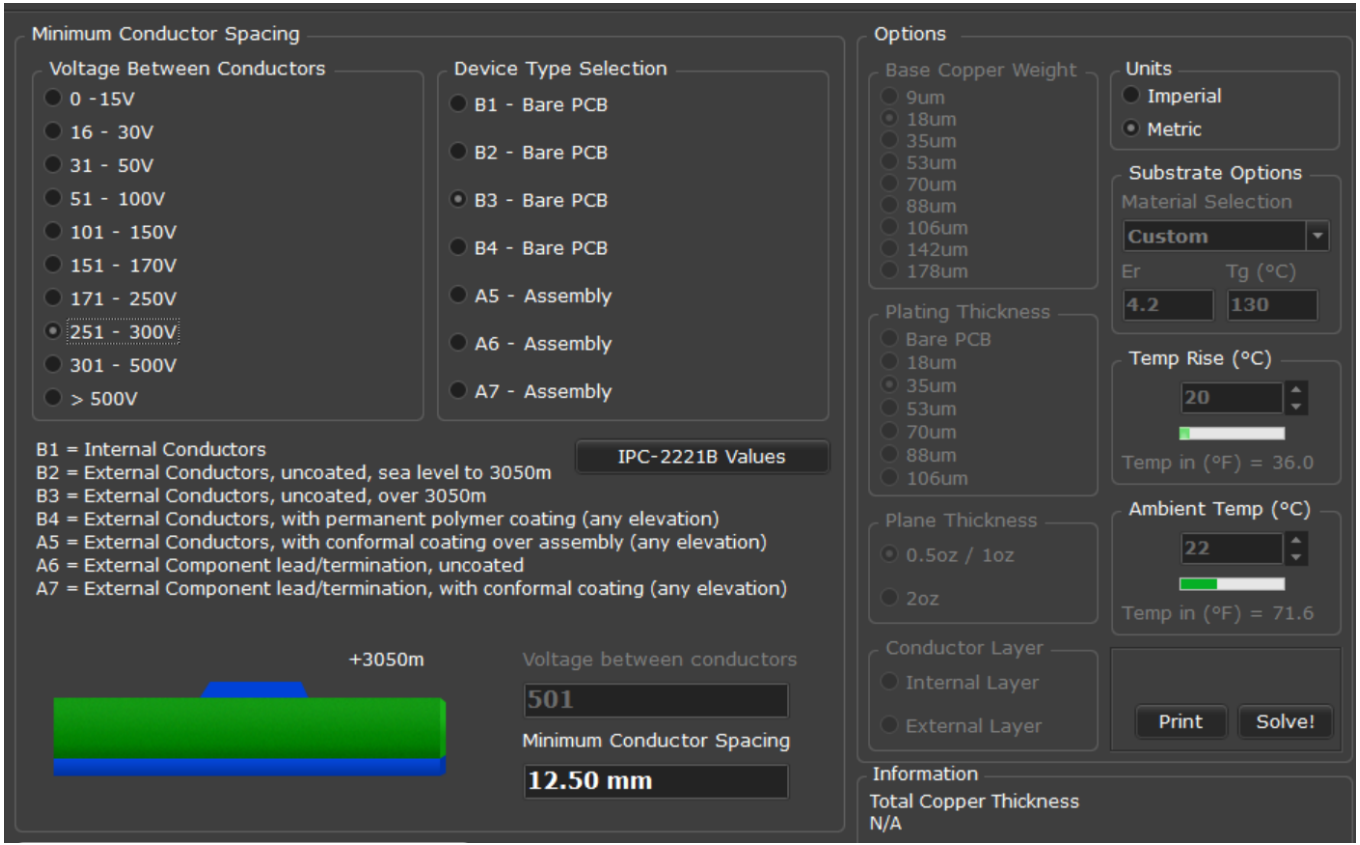
Table 6-1 Electrical Conductor Spacing

Voltage Between Conductors (DC or AC Peaks)	Minimum Spacing						
	Bare Board				Assembly		
	B1	B2	B3	B4	A5	A6	A7
0-15	0.05 mm [0.00197 in]	0.1 mm [0.0039 in]	0.1 mm [0.0039 in]	0.05 mm [0.00197 in]	0.13 mm [0.00512 in]	0.13 mm [0.00512 in]	0.13 mm [0.00512 in]
16-30	0.05 mm [0.00197 in]	0.1 mm [0.0039 in]	0.1 mm [0.0039 in]	0.05 mm [0.00197 in]	0.13 mm [0.00512 in]	0.25 mm [0.00984 in]	0.13 mm [0.00512 in]
31-50	0.1 mm [0.0039 in]	0.6 mm [0.024 in]	0.6 mm [0.024 in]	0.13 mm [0.00512 in]	0.13 mm [0.00512 in]	0.4 mm [0.016 in]	0.13 mm [0.00512 in]
51-100	0.1 mm [0.0039 in]	0.6 mm [0.024 in]	1.5 mm [0.0591 in]	0.13 mm [0.00512 in]	0.13 mm [0.00512 in]	0.5 mm [0.020 in]	0.13 mm [0.00512 in]
101-150	0.2 mm [0.0079 in]	0.6 mm [0.024 in]	3.2 mm [0.126 in]	0.4 mm [0.016 in]	0.4 mm [0.016 in]	0.8 mm [0.031 in]	0.4 mm [0.016 in]
151-170	0.2 mm [0.0079 in]	1.25 mm [0.0492 in]	3.2 mm [0.126 in]	0.4 mm [0.016 in]	0.4 mm [0.016 in]	0.8 mm [0.031 in]	0.4 mm [0.016 in]
171-250	0.2 mm [0.0079 in]	1.25 mm [0.0492 in]	6.4 mm [0.252 in]	0.4 mm [0.016 in]	0.4 mm [0.016 in]	0.8 mm [0.031 in]	0.4 mm [0.016 in]
251-300	0.2 mm [0.0079 in]	1.25 mm [0.0492 in]	12.5 mm [0.4921 in]	0.4 mm [0.016 in]	0.4 mm [0.016 in]	0.8 mm [0.031 in]	0.8 mm [0.031 in]
301-500	0.25 mm [0.00984 in]	2.5 mm [0.0984 in]	12.5 mm [0.4921 in]	0.8 mm [0.031 in]	0.8 mm [0.031 in]	1.5 mm [0.0591 in]	0.8 mm [0.031 in]
> 500 See para. 6.3 for calc.	0.0025 mm /volt	0.005 mm /volt	0.025 mm /volt	0.00305 mm /volt	0.00305 mm /volt	0.00305 mm /volt	0.00305 mm /volt

B1 - Internal Conductors
B2 - External Conductors, uncoated, sea level to 3050 m [10,007 feet]
B3 - External Conductors, uncoated, over 3050 m [10,007 feet]
B4 - External Conductors, with permanent polymer coating (any elevation)
A5 - External Conductors, with conformal coating over assembly (any elevation)
A6 - External Component lead/termination, uncoated, sea level to 3050 m [10,007 feet]
A7 - External Component lead termination, with conformal coating (any elevation)

Courtesy: Altium

Minimum Conductor spacing Using Saturn PCB



Example – Clearance requirement violation

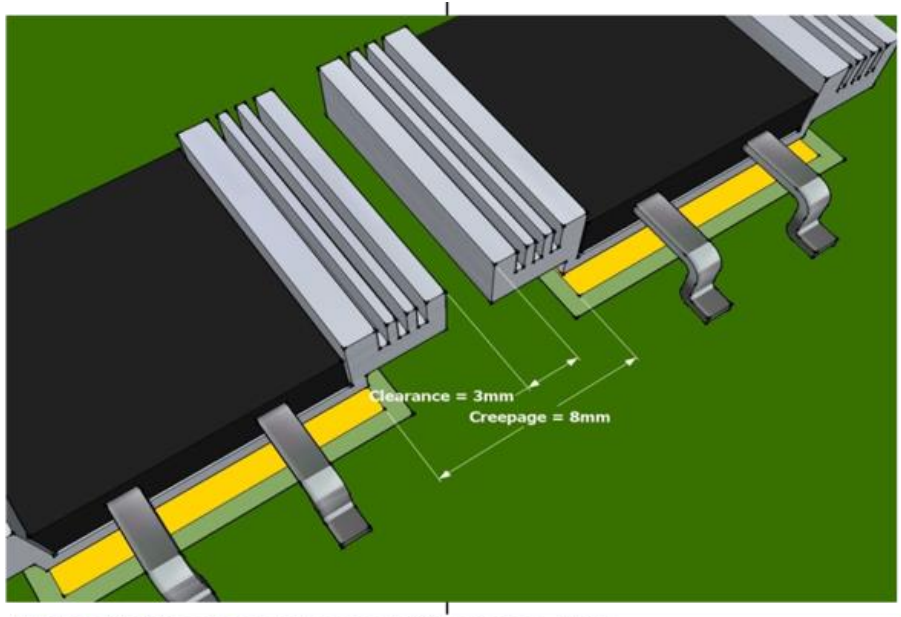


Figure 4: Creepage Passes / Clearance Fails

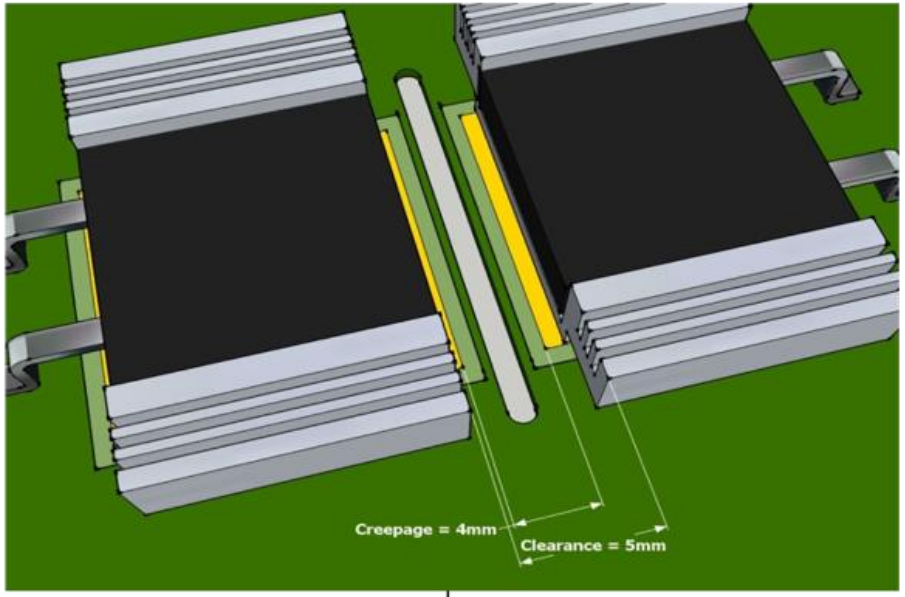
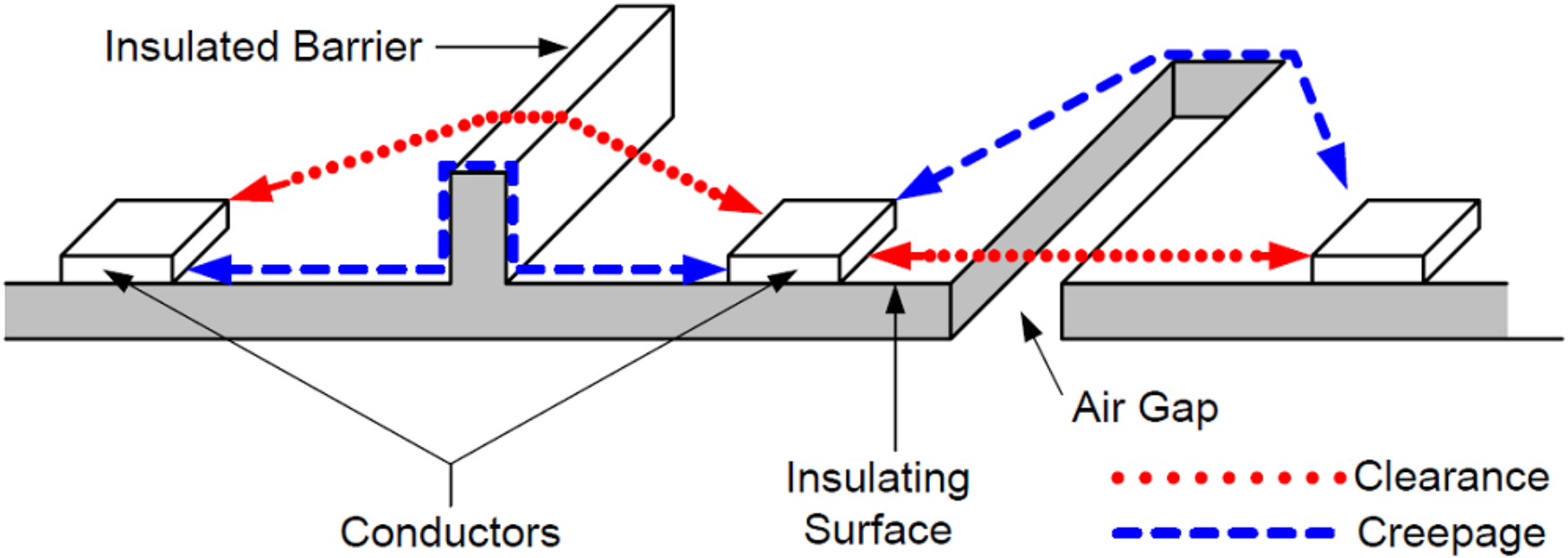


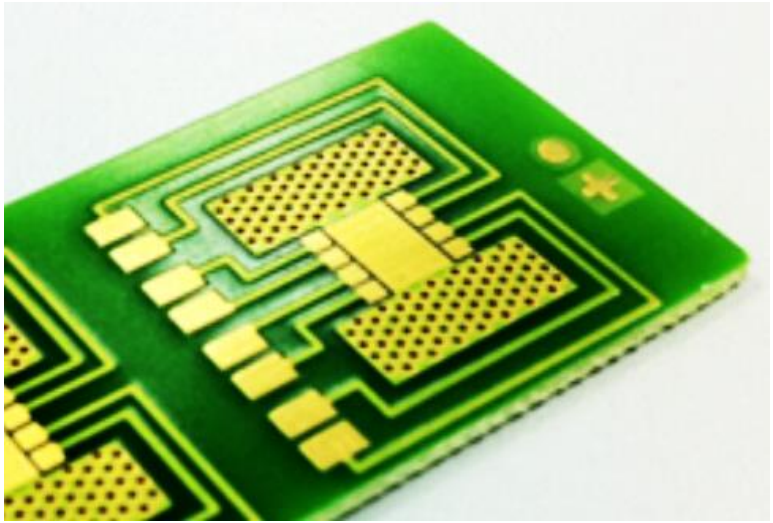
Figure 5: Clearance Passes / Creepage Fails (without slot)

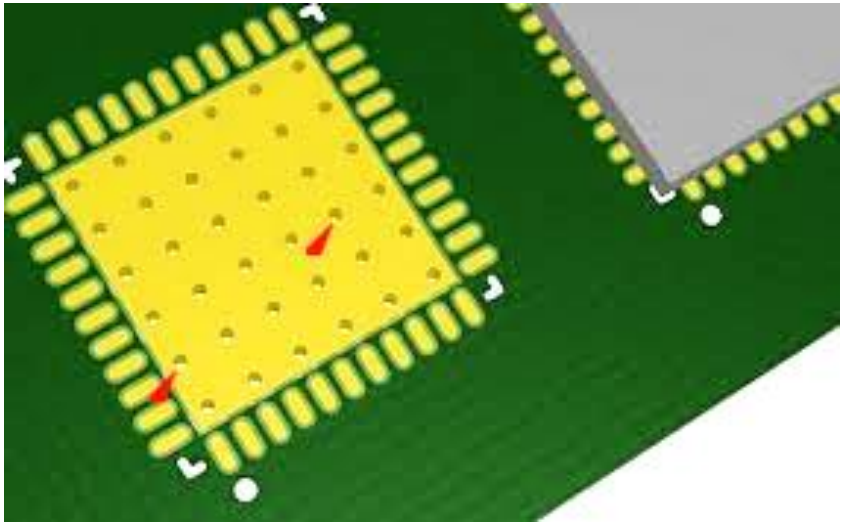
Courtesy: Optimumdesign.com

Techniques to meet clearance and creepage



Courtesy: PhilipMcGaw.com





PCB Copper Area for Thermal Management

FOR POWER DISCRETES AND ICS

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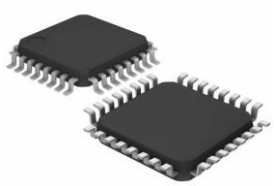
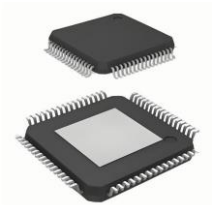
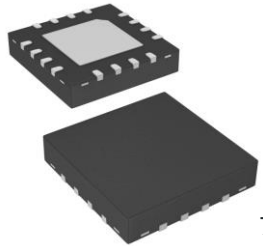
Junction temperature Tj of IC and Power devices

- **“T_j” The junction temperature** of the IC or a power discrete component, needs to be kept below its maximum value to avoid failure (125-150° C for most ICs).
- **Factors affecting T_j :** Higher the power dissipation in the IC, higher the rise in T_J. Rise in ambient temperature “T_a” results in rise in T_j.
- **Role of an IC package:** For high-power devices, the IC package plays a major role in taking out the heat from junction to the ambient so that T_j can be kept safe. Power MOSFETs typically comes with a metal tab to connect an external heatsink to take away the heat from junction and move to ambient. Even some ICs do have exposed metal pad.

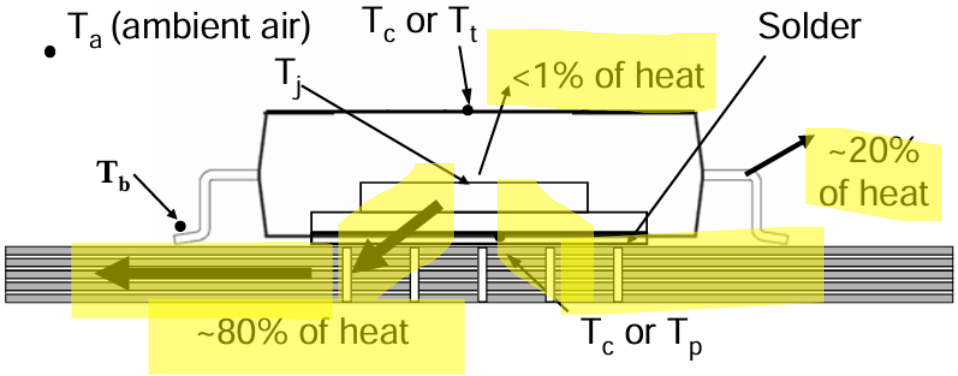


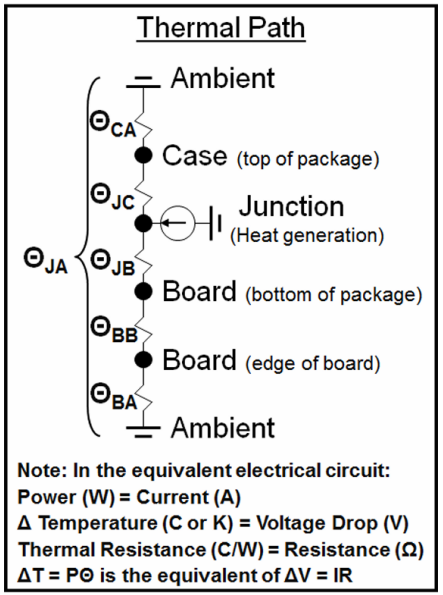



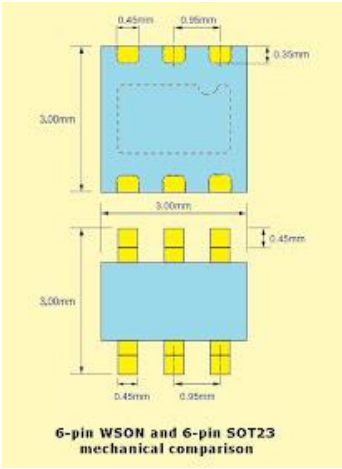




Thermal nodes and Heat flow







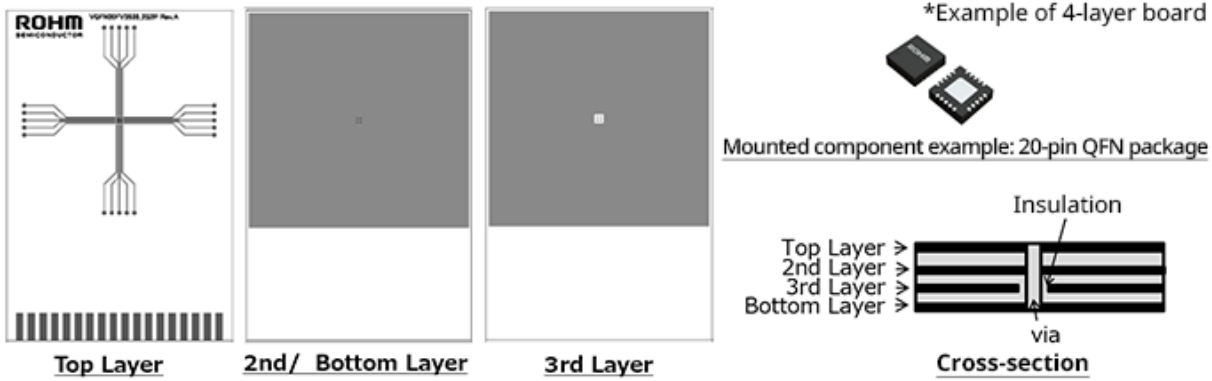
- Tj-Junction temperature of IC (IC datasheet specs);
- Tc-Casing temperature;
- Tt-Top of IC casing temperature;
- Tb-Board Temperature
- Ta-Ambient Temperature;

- If the component doesn't have exposed pad, ensure the power dissipation in the device is within limits so as not to exceed θJA limit.
- With exposed pad, there may is a possibility to reduce the θJB and θBB with PCB design

Key thermal parameters and formulas

- **Theta JA (θJA):** Total resistance from junction to air (° C/W); includes package, PCB copper, and airflow. Use for PCB-only cooling.(Given in IC datasheet)
- **Theta JC (θJC):** From junction to case of components.(Given in IC datasheet)
- **JEDEC Test standard (for θJA determination):** Measured on standard boards; multi-layer θJA ~50% lower than single-layer.(Given in IC datasheet)
- **JEDEC Specs:** JESD51-7 for high-conductivity boards; ensure design matches test conditions for accurate estimates.
- **Formulas: $T_j = T_a + P \times \theta_{JA}$** (natural convection).**$T_j = T_c + P \times \theta_{JC}$** (with heatsink; Tc = case temp).
- **Power Dissipation: $P = I^2 \times R_{ds(on)}$** (MOSFETs) or **$V \times I$** (linear regulators). In case of switching regulators, calculate the power loss from efficiency.

Thermal Standards: JEDEC 51-7 2S-2P test PCB



Demension	Value
Board finish thickness	1.60 mm
Board dimension	76.2 mm × 114.3 mm
Board material	FR-4
Trace finish thickness (Top/Bottom)	0.070mm
Trace finish thickness (2nd/3rd)	0.035mm
Copper foil area (Top)	Footprint
Copper foil area (2nd/3rd/Bottom)	74.2 mm × 74.2 mm
Therml vias separation / diameter	1.2mm / 0.3mm

Courtesy: ROHM

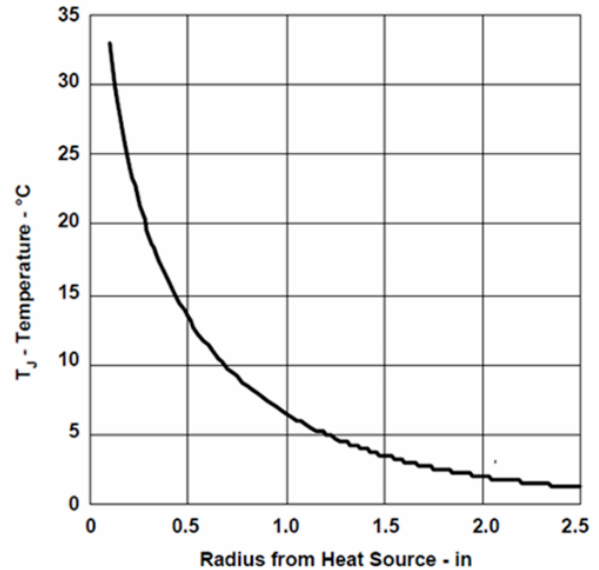
Can you really afford to have this much area of copper reserved for each IC in your PCB layout always?!

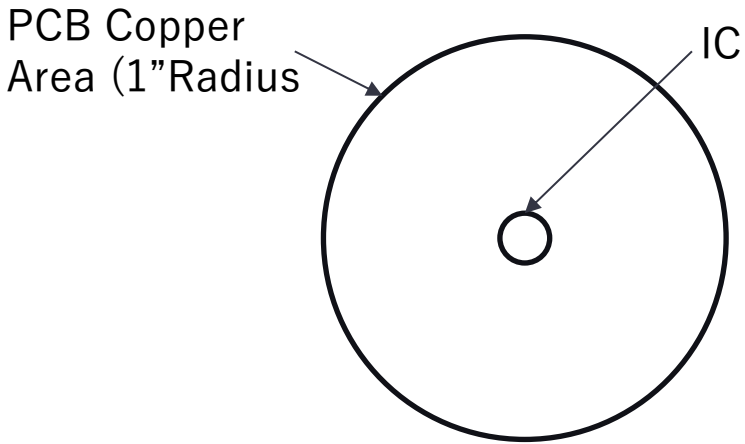
So, what is the solution?

IC Thermal Management: Deciding on PCB copper area

- **Purpose:** We need to provide necessary copper area needed on a PCB to dissipate heat from ICs/power discretes, to ensure junction temperature (T_j) stays below max spec (e.g., 125-150° C).
- **Based On:** Datasheet Theta JA (junction-to-ambient) for PCB/board-level cooling; Theta JC (junction-to-case) when using external heatsinks or using PCB area, Theta JC/JB when using components with large exposed pad.
- **Factors:** Power dissipation (P), ambient temp (Ta), board layers, vias, and heat transfer modes (conduction dominant, convection/radiation from surface).
- **Standards:** JEDEC JESD51 for θJA/θJC measurements on test boards (1S0P **single-layer; 1S2P; 2S2P multi-layer with planes).**
- **Goal:** Minimize thermal resistance (R_th) via copper area to achieve desired $\Delta T = P \times R\_th$.

Temperature distribution on the PCB surface

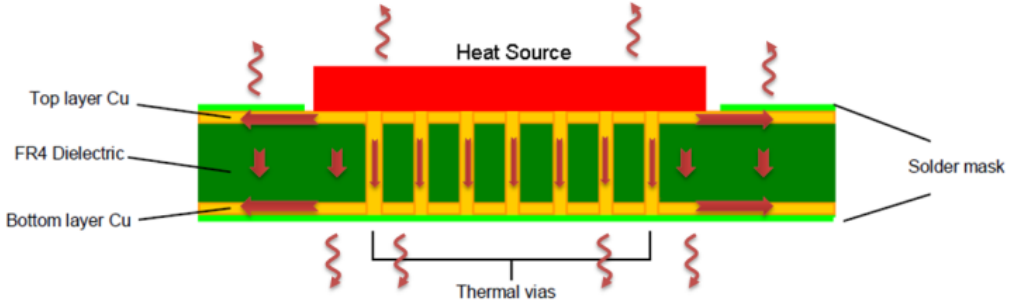


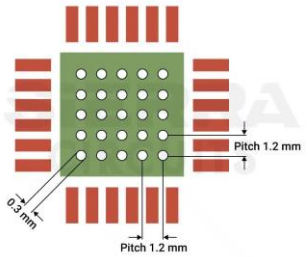


Temperature Distribution Laterally from IC Decreases Exponentially

- It is a best practice to maintain a copper area on all the layers as a circle of radius “1-inch” around the IC / discrete component having power loss .
- Good to have 2oz Cu for outer layers and 1oz Cu for inner layers.

Thermal Management: The "Heat Pipe" of PCBs

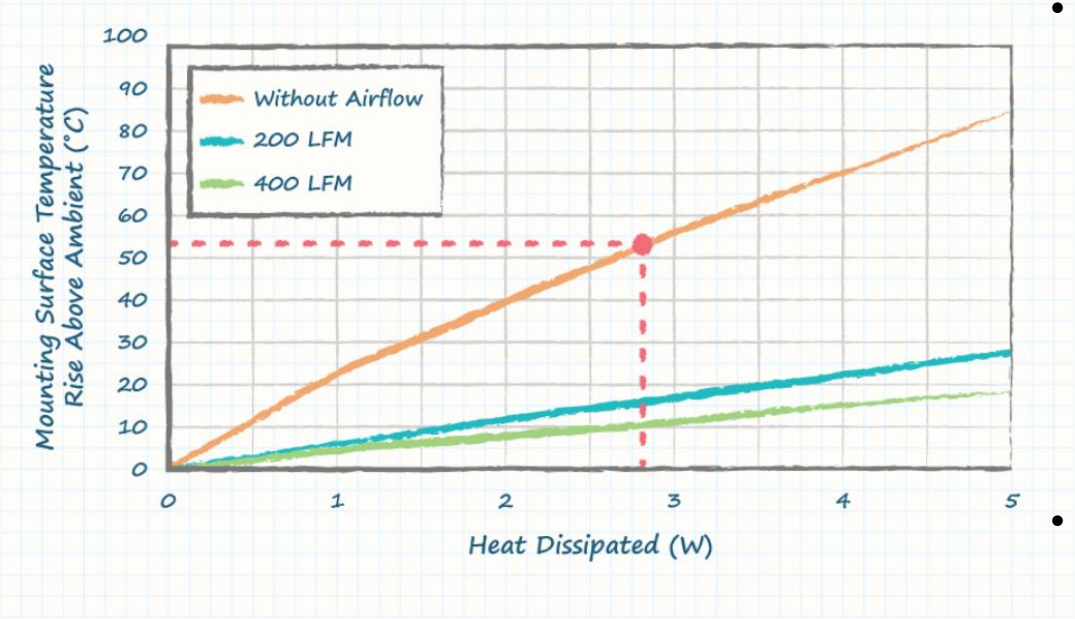




Thermal vias are small holes placed directly under the thermal pad of a component. They act as "thermal bridges" that carry heat from the hot top layer to the cooler internal or bottom copper planes.

- Hole Size: Typically**, 0.2 mm to 0.3 mm**. If the hole is too large (e.g., >0.5 mm), solder might "wick" through the hole during assembly, leaving the component pad dry (a defect called "solder voiding").
- Pitch: Vias are usually spaced **1.0 mm to 1.2 mm** apart in a grid pattern. Plating: Ensure the vias are plated-through-hole (PTH). The copper barrel of the via is what actually conducts the heat.

Thermal Management: Flow of Air



Graph showing the typical heat sink mounting surface temperature rise above ambient

- Air surrounding is a fluid and hence the heat from the PCB flows through convection on to the air surrounding it. Where there is no flow of air, the heat above the PCB is much warmer and hence it slows down further flow of heat (as the heat flow depends on the difference in heat between the PCB and the air/fluid).
- Hence having a fan can helps to move the hot air out and bring in air at lower temperature from atmosphere.

Understanding Thermal Specs of IC

THERMAL INFORMATION

THERMAL METRIC (1) (2)		TPS74001DGK	TPS74001DPT (3)	UNITS
		DGK (4 pin short)	DPT	
		8 PINS	5 PINS	
θ_{JA}	Junction-to-ambient thermal resistance (4)	136.9	30.0	°C/W
θ_{JCtop}	Junction-to-case (top) thermal resistance (5)	35.3	15.3	
θ_{JB}	Junction-to-board thermal resistance (6)	68.0	14.4	
ψ_{JT}	Junction-to-top characterization parameter (7)	0.9	0.6	
ψ_{JB}	Junction-to-board characterization parameter (8)	67.8	14.4	
θ_{JCbot}	Junction-to-case (bottom) thermal resistance (9)	n/a	5.8	

- From the given θ JA value, lets calculate Tj of the device. ($Tj = Ta + P \times \theta JA$)
- Assuming Ta = 25degC, Power loss P on the device = 1W, Tj = 161.9degC for DGK pack and Tj = 55degC. So, if the power loss in the device is 1W, then we can only use TPS74001DPT safely (Cannot use TPS74001DGK)

Nuances of IC thermal spec and it's influence on PCB

(3) Thermal data for the DGK and DPT packages are derived by thermal simulations based on JEDEC-standard methodology as specified in the JESD51 series. The following assumptions are used in the simulations:
(a) DPT only, the exposed pad is connected to the PCB ground layer through a 8 × 8 thermal via array.
(b) i. DPT: Each of top and bottom copper layers has a dedicated pattern for 20% copper coverage.
ii. DGK: The top copper layer has a dedicated pattern of 5% copper coverage and the bottom copper layer has another decicated pattern of 20% copper coverage.
(c) These data were generated with only a single device at the center of a JEDEC high-K (2s2p) board with 3in × 3in copper area.
(4) The junction-to-ambient thermal resistance under natural convection is obtained in a simulation on a JEDEC-standard, high-K board, as specified in JESD51-7, in an environment described in JESD51-2a.

- Carefully reading the data sheet, we can understand that the thermal spec is derived by mounting the IC on JEDEC high-K 2s-2p board with 3inch x 3inch copper area(4 Layer board).
- So, this θJA value is applicable only if our PCB has similar copper area available for the IC !
- If the copper area allocated for the IC is less, then the temperature rise is going to be higher.

Thermal Management: Application notes

- ROHM: Basics of Thermal Resistance and Heat Dissipation
- ROHM: How to Use the Thermal Resistance and Thermal Characteristics Parameters
- Same Sky Devices: How to select a Heatsink
- TI: Accurate Thermal Calculations on the Back of a Napkin
- TI: LDO Thermal Performance
- TI: AN-1520 A Guide to Board Layout for Best Thermal Resistance for Exposed Packages
- TI: AN-2020 Thermal Design By Insight, Not Hindsight
- ADI: Analyzing IC Heat Dissipation? Forget the Software Modeling, Use Your Pencil!
- RICHTEK: Application and Definition of Thermal Resistances on Datasheet
- TI-MOSFET power loss calculator for motor drive applications

Ground Planning

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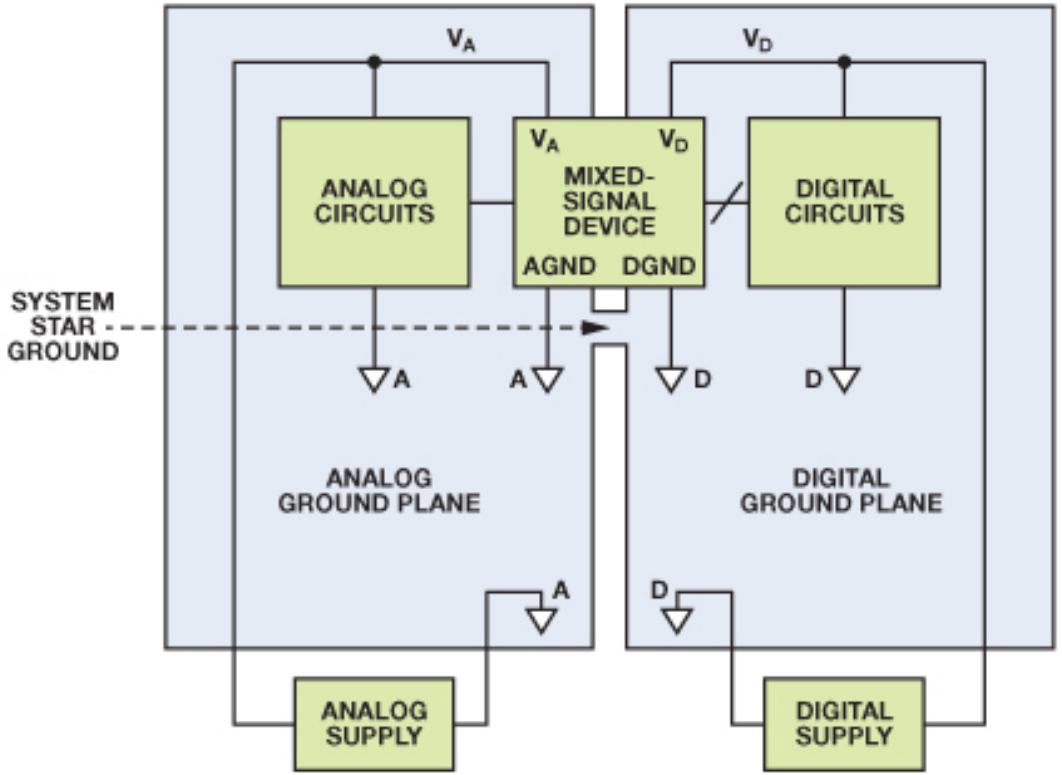
Ground planning in mixed signal PCBs



The analog parts of your board need to be kept separate. This includes analog-to-digital converters and digital-to-analog converters.

When designing the “floor plan” of your PCB, be sure to keep these areas isolated.

An ADC’s ground can be tied back to a common ground point where digital signals can be passed to other parts of your PCB.

IPC Standards

PRINTED BOARD
IPC-2141
IPC-2152
IPC-2221
IPC-2222
IPC-2223
IPC-2225
IPC-2226
IPC-2251
IPC-2252
IPC-2611
IPC-2612
IPC-2612-1
IPC-2614
IPC-2615

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IPC Standards

- IPC standards enable reliable, high-quality electronics by developing the **trusted standards that drive the global electronics industry's success.**
- Implemented industry-wide, IPC standards simply communicate and clarify expectations for everyone within the industry.
- **IPC standards help ensure superior quality, reliability and consistency in electronics manufacturing.**
- There are over **300+ active IPC multilingual industry standards covering nearly every stage of the electronics product development cycle**.
- More than 3,000 electronic industry professionals are participating in the development of these standards.

IPC Standards for Rigid FR4 PCB

Design & Layout (The "Blueprint" Standards)

These dictate how you actually draw your board in any of the PCB design software.

- **IPC-2221:** The "mother" of all design standards. It covers everything from trace clearance (creepage) to material properties.
- **IPC-2222:** Specifically for Rigid Organic Printed Boards (standard FR-4). It provides formulas for calculating trace width based on current and heat rise.
- **IPC-7351:** Requirements for Surface Mount Design and Land Patterns. This ensures your footprints (pads) are the right size for the components to be soldered properly without shifting or "tombstoning."

Manufacturing & Quality (The "Acceptability" Standards)

These define what a "good" board looks like after it comes off the assembly line.

- **IPC-A-600:** Acceptability of Printed Boards. This is for the bare board fabrication. It defines what constitutes a defect in the FR-4 laminate, copper plating, or solder mask.
- **IPC-A-610:** Acceptability of Electronic Assemblies. This is the most widely used standard in the world. It sets the criteria for solder joints—defining what is a "Target," "Acceptable," or "Defect" joint.

IPC Performance Classes

IPC categorizes products into three classes. As an engineer, you must decide which class your board falls into:

Class	Description	Examples
Class 1	General Electronic Products	Toys, TV remotes (Short life, low cost).
Class 2	Dedicated Service Products	Laptops, Industrial equipment (Long life, continuous use).
Class 3	High Reliability/Harsh Environment	Medical life support, Aerospace (Failure is not an option).

If you are designing PCB for a client, the first question you should ask is: **"Are we designing to IPC Class 2 or Class 3?"** This single answer determines your minimum trace spacing, annular ring sizes, and testing requirements.

The "Must-Know" IPC Table for FR-4 Layout

Topic	IPC Standard	Why it matters to you
Trace Width	IPC-2152	Determines if your trace will burn out under high current.
Clearance	IPC-2221	Prevents high-voltage "arcing" between traces.
Vias	IPC-4761	Defines how to tent or plug vias to prevent solder wicking.
Stackup	IPC-4101	Specification for the FR-4 material itself (Tg, dielectric constant).

Ex: IPC Training Calendar

IPC offers paid training and certification programs worldwide

Course	Endorsement Program	Date	City	Mode of Training
IPC J-STD-001H	Requirements for Soldered Electrical and Electronic Assemblies	Jan 2 - 6	Bengaluru	Live Classroom Training with Hands on Practical Session
IPC-A-610H	Acceptability of Electronic Assembly	Jan 8 - 11	Hyderabad	Live Classroom Training
IPC/WHMA-A-620E	Acceptance for cable and wire Harness Assemblies	Jan 8 - 12	Bengaluru	Instructor Led Virtual/Classroom with /without Hands on Practical Session
IPC/WHMA-A-620E	Acceptance for cable and wire Harness Assemblies	Jan 15 - 19	Pune	Live Classroom with Hands on Practical Session
IPC-CID (Basic)	PCB Designer - Individual	Jan 18 - 20	Bengaluru	Instructor Led Virtual/Classroom Training
IPC-A-610H	Acceptability of Electronic Assembly	Jan 22 - 25	Pune	Live Classroom Training
IPC-A-610H	Acceptability of Electronic Assembly	Jan 22 - 25	Bengaluru	Instructor Led Virtual/Classroom Training

Summary

- Try to visualize the coupling capacitances, trace inductances, and resistances. Always use calculators to validate intuition. Try to use free simulation tools such as LTspice to understand how it may affect your design.
- Always think where current flows, think of return paths and know the loop size.
- Be aware of nodes where the voltage swings to a large amount.
- Never forget to calculate power losses in components and ensure thermal design is done to extract the heat out to ambient.
- Keep the Ground plane continuous and use vias to stich all grounds.

Key Takeaways

- PCB design is a **core engineering skill, and it is as important as the schematic / circuit design**
- PCB layout determines system behavior and product success
- Tools are good but are secondary to principles
- Good PCB design is invisible, Bad PCB design is expensive
- **Engineering thinking is a must for PCB design**

Let’s build things right at first time!

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